Predict differential conducted EMIs with a SPICE simulator

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The classical method used to quantify conducted EMI disturbances of switched mode power supplies (SMPS) consists of evaluating the level of the perturbing signal generated by the power supply under test. To simplify the calculation, the SMPS signature is approximated by a recurrent square wave associated with its rise and fall times. Despite the correct estimation given by the procedure, the differential signal delivered by some topologies can be very far from this assumption. The first option is to precisely calculate the Fourier transform of each original signature. Depending on the operating parameters (line level, load, conduction mode, etc) however, one has to perform the calculation for every condition. In this article, we show how a SPICE simulator can help to analyze the precise behavior of any particular power structure and give first assessments of future differential EMI results.

How a parasitic signal is generated

Figure 1a, represents a simple off-line power supply, regardless of its inherent topology. The transistor is activated by an external pulse width modulator (PWM) integrated circuit and chops at high frequency the current inside the primary inductor.

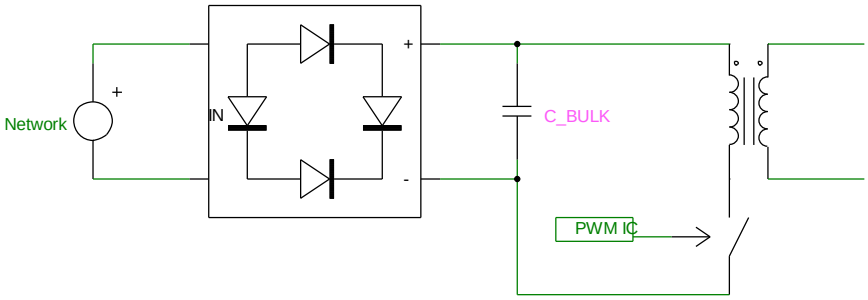


Figure 1a

All the energy is provided by the bulk capacitor C_BULK, because of the period difference between the mains and the switching action. C_BULK is re-charged at a low rate by the electrical network and if we consider its impedance to be very small and negligible at high frequencies, then the equivalent model of the whole circuit is shown as **figure 1b**.

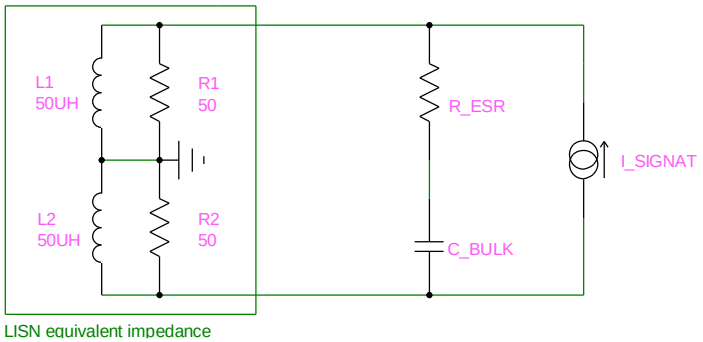


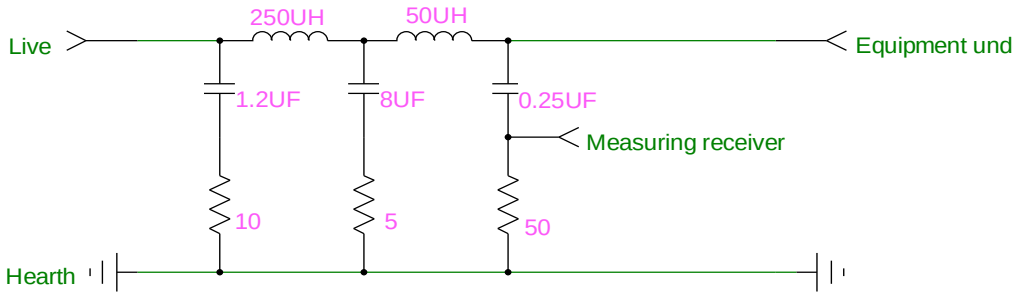
Figure 1b

The current flowing inside the inductor is replaced by an equivalent current source whose shape corresponds to the SMPS signature. The capacitor can be replaced with its equivalent series resistor (ESR) and, for switch cycles under 1µs, the designer can add the equivalent series inductance (ESL, 20 nH typically for a 47-µF 400-V snap-in). However, one should keep in mind that the equivalent series representation of a capacitor has elements that are frequency, bias and temperature dependent. An accurate model should account for all these contributions but may be too computationally intensive for some applications. For those who want to include the equivalent series capacitance in their capacitor model, manufacturer C/C_0 curves provide the capacitance value at the operating frequency (C_0 = the capacitance at 20 °C and 100 Hz). The ESR value can be extracted from

the ESR/ESR$_0$ curves, which depict the variations of this ratio versus frequency (ESR$_0$ = the ESR at 100 Hz and 20 °C).

A complete capacitor model is described in the November 1995 and January 1996 INTUSOFT Newsletter. It illustrate the way to accurately model a capacitor with temperature, frequency and bias dependent elements.

The bridge diodes are assumed to conduct all the time at these high frequencies and are represented by a short circuit. The final measurement will be carried over a Line Impedance Stabilization Network as defined by CISPR 16 (**figure 1c**).



Same network for other phases or neutral

Figure 1c

This network is mainly dedicated to (a) maintaining a known RF impedance at the measuring points during a frequency sweep analysis, (b) isolating the device under test from incoming perturbations, and (c) routing the noise components to the spectrum analyzer. The CISPR 16 LISN impedance starts from nearly 5 Ω at 10 kHz and rises to a constant 50 Ω above 1 MHz. In our model, this circuit consists of two simple 50-Ω sense resistors in parallel with 50-µH LISN coils. 5-Ω resistors could also be added in series with these coils. By circulating inside the ESR (or the whole capacitor model), the SMPS current generates a noise voltage. This noisy voltage is superimposed on the main rectified DC rail. It then gives rise to a sense signal across both 50-Ω resistors. To reduce this noise below the EMC standard limits, the designer needs to install a filter that will isolate the mains from its polluter. The final sketch is given in **figure 1d**.

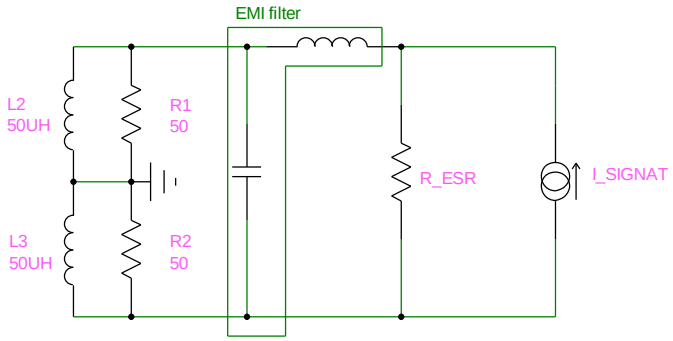


Figure 1d

Evaluating and correcting the level of harmonics disturbances

If we take a classical square wave signal, with a duty ratio D, a peak value I_p and finite rise time t_r, as a starting point, we can calculate the corresponding Fourier coefficients. The well-known result for the fundamental is:

$$I(fund) = 2 \cdot I_p \cdot D \cdot \frac{\sin(\pi D)}{\pi D} \cdot \frac{\sin(\pi\, t_r/T)}{\pi\, t_r/T} \quad [1]$$

Suppose that we want to fulfill the FCC Part 15 class B rules, which requires that the noise level stays below a flat line at the 48-dBµV level, ranging from 450 kHz up to 30 MHz. For example,

let's say we have a SMPS producing a 300-mA peak current characterized by a 25-ns rise/fall time and a 50% duty cycle, into a 100-mΩ ESR resistor. The frequency is 800-kHz. To reduce the quantity of harmonics, we must calculate the necessary attenuation ratio that will keep the final measured level under the normalized curve. To simplify the calculations, we will assume that the sum of the ESR and series resistance of the filtering coil is small compared to the 50-Ω sense resistors (< 1%). In this case, the LISN 50-µH coils can be omitted because their value no longer modifies the impedance curve at our 800-kHz operating frequency.

Lets split the calculation into successive steps:

1. Evaluate the fundamental current from the previous formula [1]: 200 mA peak
2. Convert the fundamental current a into voltage using the capacitor's ESR: I_{peak} x ESR = 20 mV
   Transform this voltage level in dBµV: 20 **.** LOG (0.02 x 1E6) or 20 **.** LOG (0.02) + 120, giving 86 dBµV.
3. Select a target level and deduce the desired attenuation level: 48 dBµV is the maximum level imposed by FCC 15 part B. If we take 40 dBµV as a maximum level, including a safe margin, we obtain the required attenuation: 86 - 40 = 46 dB
4. Calculate the corner frequency (f_c) of the *LC* filter that will lead to a 46-dB attenuation at 800 kHz: - 46 = - 40 **.** LOG (800k / f_c) ----> f_c = 56.6 kHz
5. Select a X2 capacitor of 100 nF (not bulky, low-cost)
6. From $f_c = 1 / 2 . \pi . \sqrt{LC}$, extract the value of L: 79 µH
7. Select an inductor with this minimum inductance value up to the 300-mA peak current

In this example, we wish to stay within the limits imposed by the FCC. By evaluating and tailoring the level of the fundamental to stay within these limits, we automatically reduce the level of the remaining higher harmonics to a safe value, since the FCC specification is flat along the analysis bandwidth. However, for the defunct VDE0871 class A/B or even CISPR15, for lighting applications, we have a much more complex curve. If we take a ballast operating at 33 kHz, its fundamental at an arbitrary 90 dBµV value could be inside the open window between 10 to 50 kHz (CISPR15). However, it is clear that the higher order harmonics would be outside the rest of the authorized levels. Therefore, if we stick to the first method, we will be lead to an impractical component selection. In addition, the current shape of a ballast is very different from that of a simple square wave.

Fast Fourier Transforms with SPICE

SPICE can evaluate the harmonic levels in several ways. The **.**FOUR directive performs a classic harmonic decomposition over a period and gives results up to the harmonic 10. Unfortunately, the user can not visualize the calculations with a graphic interface.

The Fast Fourier Transform function of a SPICE graphic processor usually implements the Sande-Tooke algorithm. The algorithm evaluates the harmonic coefficients from an array consisting of a binary radix of data points (128, 256 ...). Depending on the software editor, the processing method can differ, as we will see below.

During the simulation, SPICE continuously modifies its internal time step to provide accurate results. The time step can either be shorter or longer than TSTEP, depending on the activities of the computed signals. Generally, the minimum time step can not drop below 10E-9 times TMAX but this boundary also depends upon the proprietary SPICE algorithm. Without specification, TMAX is fixed at (TSTOP-TSTART) / 50. At the end of the simulation, some SPICE simulators, as IsSpice from INTUSOFT (San-Pedro, CA) invokes, before storing the data, a linear interpolation algorithm to produce an evenly spaced output at a TSTEP interval. The results are placed in an ASCII SPICE compatible output file that can be examined with the IntuScope investigation tool. However, IntuScope also offers the ability to explore the raw simulated data.

MICROSIM's PSpice (Irvine, CA) does not interpolate the data in its **.**DAT file and the user navigates through the raw acquisitions via the PROBE graphical interface. When the FFT algorithm is initiated, PROBE first interpolates the data to convert the unevenly spaced acquisitions into fixed time step data. It then places the new acquisitions into a data array of the nearest binary radix of points, e.g. 128 locations for a 100-point simulation. PSpice can also produce an ASCII output file with interpolated data points but, in this case, the user must specify the nodes to be saved with the appropriate **.**PRINT statement in the netlist file (**.**CIR).

The maximum frequency available from the interpolated data array can not exceed the Nyquist criterion, Fmax = 1 / (2**.**TSTEP). If higher frequencies are present during the simulation, e.g. because

of a parasitic oscillation, they would incorrectly appear as lower frequencies when displayed with a graphical interface. Variable time step simulators like SPICE are equivalent to sampling systems. If the time step becomes too large, aliasing problems will occur and the linear interpolation algorithm will lead to inaccurate results. To circumvent this problem, you should clamp down on the maximum internal time step by setting TMAX to between 1/2 or 1/4 of the TSTEP value. If TMAX is too small the simulation will be unnecessarily long. If TMAX is too large or not set at all, data aliasing problems can occur.

CISPR16 and SPICE

CISPR16 specifies four measurement bands ranging from 10 kHz to 1 GHz. The bands that are of most interest to us are bands A (10 kHz to 150 kHz) and B (150 kHz to 30 MHz). The standard specifies two different analysis filters to sweep the spectrum from A to B. In range A, the measuring instrument uses a filter whose bandwidth is 200 Hz (6dB). In range B, the instrument filter toggles to a 9 kHz bandwidth (6 dB). Depending on the target compliance curve, the spectrum sweep will be performed with different detectors types: peak, quasi-peak or average. For example, VDE0871 is specified for quasi-peak detection which accounts for weighted charge and discharge time constants. If the sweep succeeds with a peak detector, it will automatically pass the quasi-peak test which always delivers a lower output voltage. By modifying the analysis bandwidth during the sweep, the energy encompassed by the filter will change, leveling the noise floor accordingly. Thus, when switching from 200 Hz to 9 kHz, the noise floor grows by a factor of 16.5 dB.

To illustrate this, consider a simulation lasting 100 µs in which the user saves the data to an ASCII output file by specifying a TSTEP value of 1 µs. This results in 100 data points. When launched under the graphical interface, the FFT algorithm will first interpolate the data if it has not already been performed, and then create an array made of 128 locations in which the new interpolated data points will be placed. The time interval becomes: 100 µs / 128 = 0.78 µs. With this new time interval, the displayed analysis bandwidth is truncated to 1 / (2 . 0.78 µs) or 640.2 kHz. Finally, in its time to frequency conversion process, the graphical processor places half the data points in a real array and half the points in an imaginary array. The result from this example is then 64 points. The frequency resolution is 1 / 100 µs or 10 kHz. This last value also defines the analysis filter which is centered at 10 kHz. Some graphical processor allows the user to build time windows (Hanning, Hamming ...) in order to reduce the spectral leaks. If a Hanning window has been built over the 100 µs temporal block the width is 10 kHz at -6 dB.

Normally, for accurate comparisons between simulated and real plots, the simulation time should be adjusted in order to match the normalized CISPR16 filter bandwidth at -6 dB (200 Hz and 9 kHz). But to simplify the various timing values and limit the number of simulated data points, 500 Hz and 10 kHz will be used as analysis bandwidths

Analysis bandwidths

With a SPICE simulator, it is impossible to modify the time step resolution accuracy during a transient run. Nevertheless, you can run multiple transient analyses corresponding to the bandwidth you want in separate windows and then use the copy/paste function upon a common window. The lines below give the SPICE transient commands you can use to obtain various analysis bandwidths:

.TRAN TSTEP TSTOP [TSART] [TMAX] [UIC] [optional]

.TRAN 100NS 801US 400US 50NS UIC ; 5.2 MHz sweep range, 2.493 kHz analysis BW, 4010 points [2]
.TRAN 24.44NS 500US 400US 12.22NS UIC ; 20.48 MHz sweep range, 10 kHz analysis BW, 4091 points [3]
.TRAN 489NS 2.1MS 100US 244.5NS UIC ; 1.024 MHZ sweep range, 500 Hz analysis BW, 4090 points [4]

Multiple transient runs can be quite time consuming. For low switching frequencies (up to 100 kHz), a compromise can be found by using a 2.5 kHz frequency step associated with a 5.2-MHz sweep range. This allows you to quickly run and modify the design.

SPICE simulates the exact current signature

We want an exact signature of the power system under test in order to see how the filter diminishes the polluting harmonics. A plot of the target standard displayed over the final waveforms will clearly demonstrate if the calculation failed or succeeded.

Figure 2 shows an off-line flyback SMPS delivering 1 A to a resistive load from a 230-V rms rectified network. The heart of the circuit is an INTUSOFT UC1843 model that can be replaced by any other equivalent switched model. The supply operates discontinuously and uses the current mode technique. The UC1843 drives a high-voltage MOSFET whose drain is protected against leakage inductance effects by a clipping network. The current signature is simulated by the controlled current source F1 which routes the primary current into R_ESR and generates the corresponding noisy voltage. The ESR value is taken from the manufacturer's data-sheet of your tank capacitor at the operating frequency (ESR/ESR_0 curves). You can even draw the complete ESR + C + ESL network. The rest of the circuit is a direct copy of the previously described model. The final sensed value is extracted from the voltage across RSENS1 and 2 (VSENSE1).

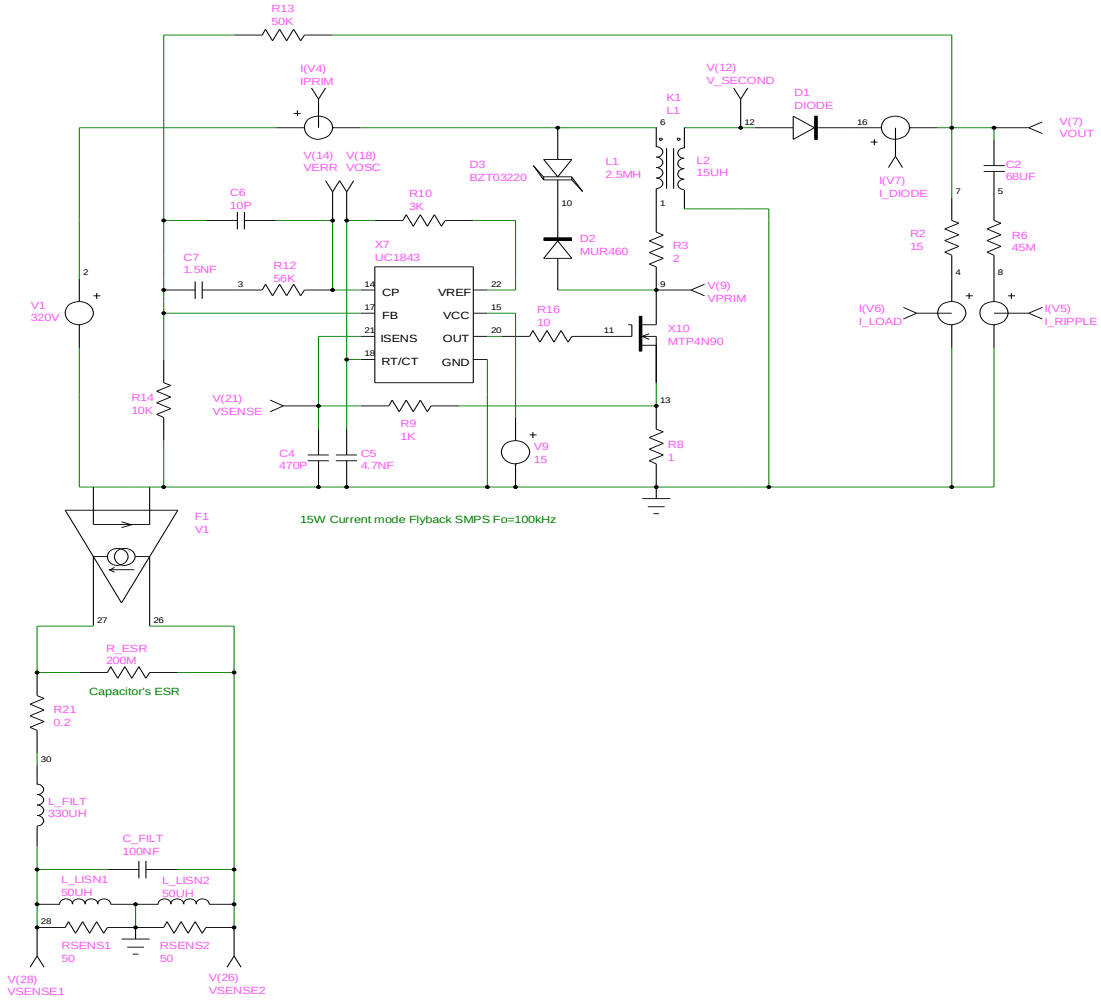


Figure 2

The simulation is run in two steps: first, the L_FILTER C_FILTER elements of the schematics are replaced by low values, such as 1 nH and 1 pF. This eliminates them from the simulation and gives the simulated harmonic level generated by the equipment under evaluation. Then replace the *LC* filter elements with the calculated values and start a new simulation to see if the final result corresponds to what you are looking for. In both cases, once the simulation is completed, you can perform the FFT upon the VSENSE1 voltage to get the EMI plot as shown on **figure 3**.

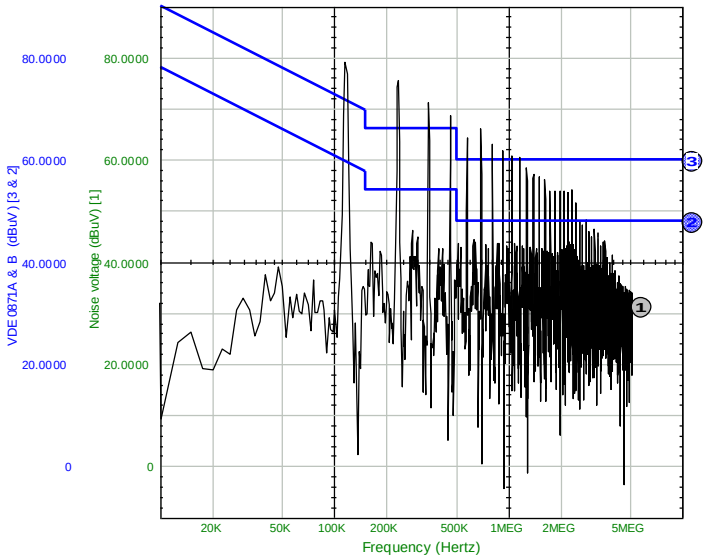


Figure 3

This plot sweeps from 10 kHz up to 5 MHz with a 2.5-kHz resolution bandwidth.

The designer can immediately evaluate the level of harmonics produced by his simulated SMPS and check if it complies with the standard's requirements to be fulfilled. After identifying the guilty harmonics, the next step is to calculate the required attenuation that leads to a successful final level across the two sense resistors. You should run the simulation until the correct result is obtained (**figure 4**).

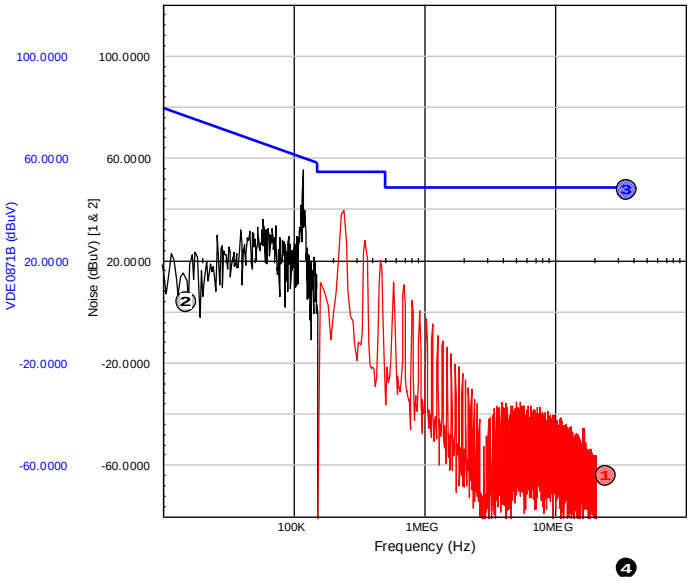


Figure 4

Once successfully completed, SPICE lets you modify the operating conditions such as the overload, line variations, etc and check if the resulting filter is still efficient. If available, the power cord elements can also be added to the whole model to reveal any annoying resonance.

Simulate and correct an electronic ballast

The schematics of our 32-W ballast is given in **figure 5**.

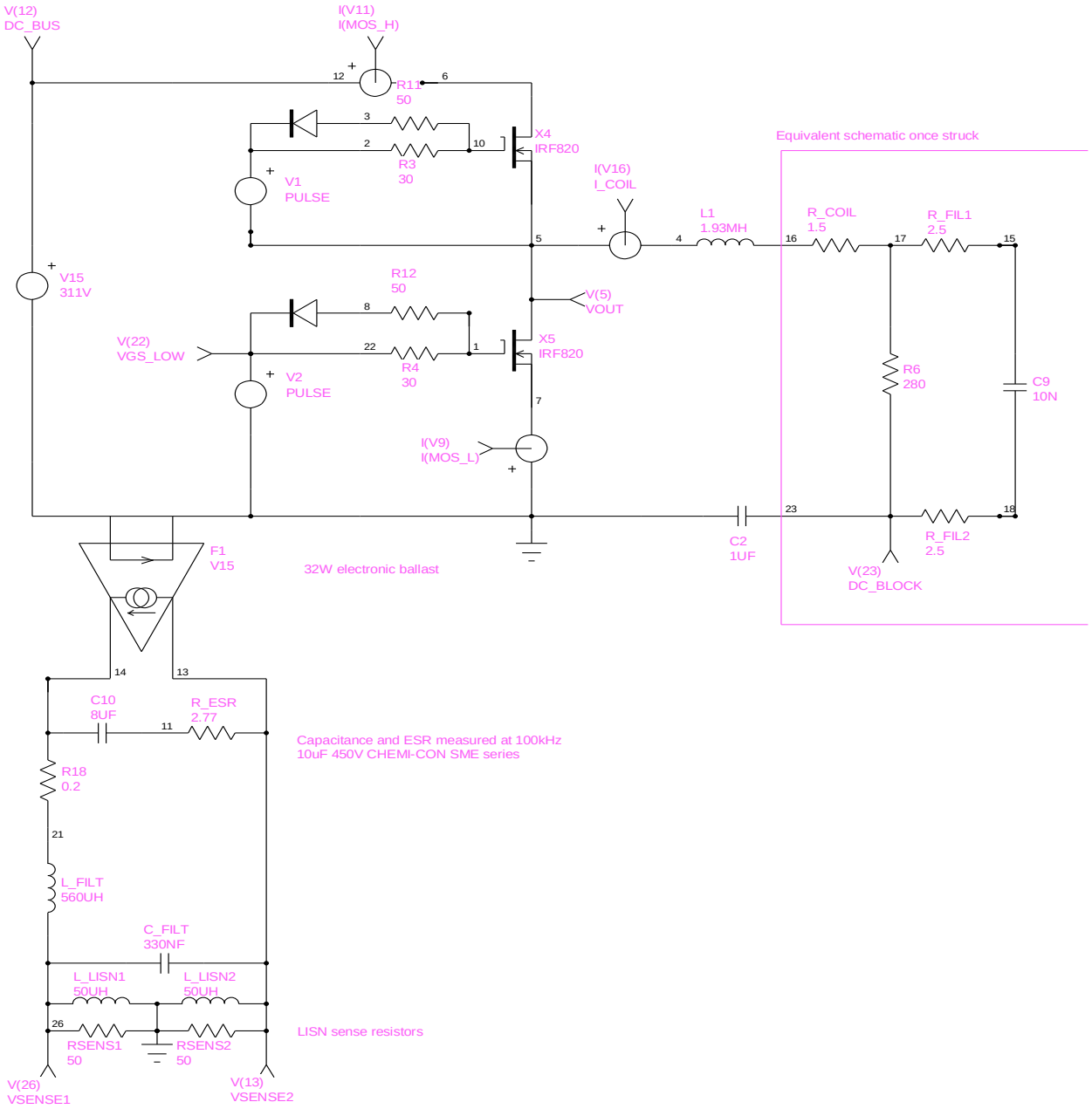


Figure 5

It shows a half-bridge configuration, typically driven by a dedicated integrated circuit such as the IR2155 from International-Rectifier (EL-SEGUNDO, CA) which implements a bootstrap technology. The main frequency is around 33 kHz with the internal dead-time set at 1.5 µs. The circuit delivers square waves that drive an *LC* circuit strongly damped by the active fluorescent tube. The tube can be represented by its equivalent resistive behavior, which is weakly capacitive. To make the tank resonate at power-on, capacitor C_9 tunes the *LC* network and provides the high-voltage spike necessary to start the tube. **Figure 6** depicts the most important curves of the whole operating circuit, especially the current flowing through the capacitor's ESR.

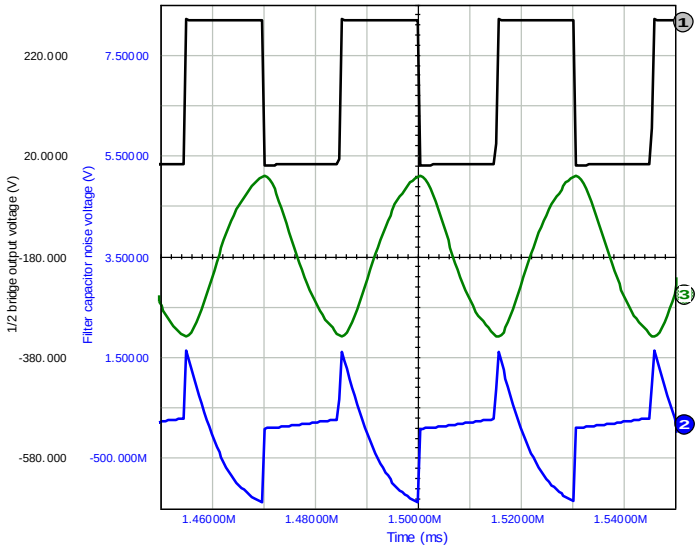


Figure 6

To show the harmonic content of the parasitic signal, display the VSENSE1 voltage and launch the FFT algorithm. If you superimpose upon the graphics the CISPR 15 compliance curve, specially dedicated to lighting applications, you can immediately see that the level of parasitic noise is much too high. Note that the fundamental of the switching frequency is roughly within the limits (**figure 7a**).

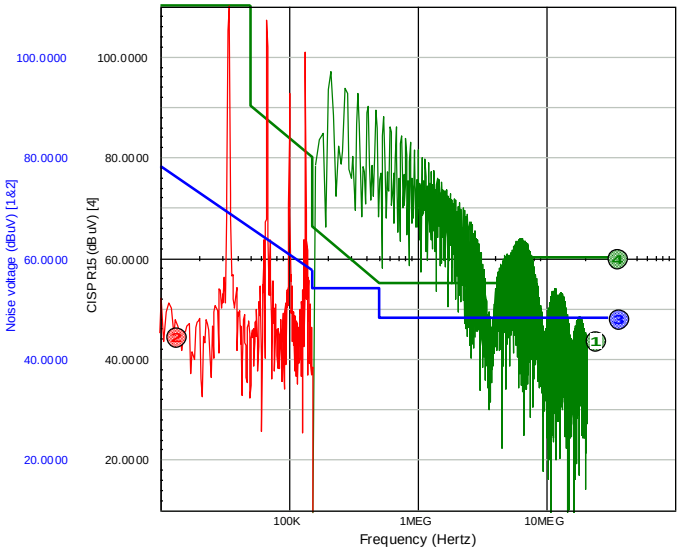


Figure 7a

The DC output component is limited by the 0.47 µF capacitor C_2. To limit the amount of ac flowing in C_{10} thus elevating its temperature with the corresponding ESR losses, you could add another capacitor with the same value as C_2 from node 23 to node 6 (dc rail). As we would expect, the amount of noise across C10 should be lower, thus reducing the generated parasitic noise. Unfortunately this is wrong, as the **figure 7b** demonstrates! The new filter capacitors produces a resonating filter which emphasizes the second harmonic amplitude and lead to a much higher noise spectrum.

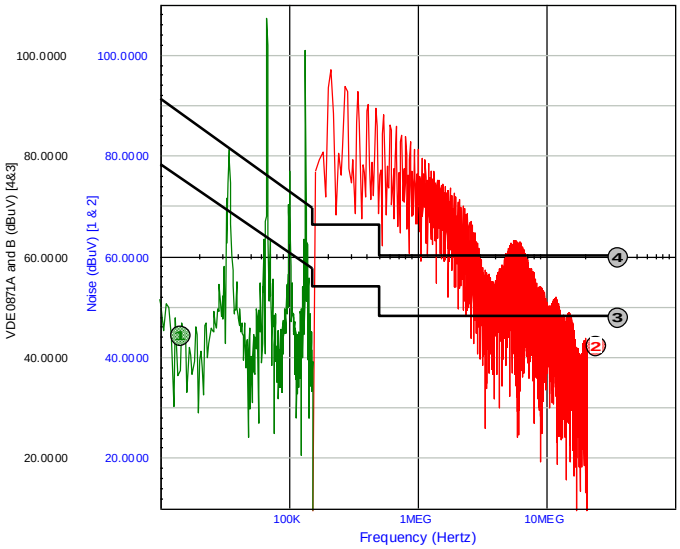


Figure 7b

Using the method we describe in the beginning of the article, determine the proper filter to be installed and run the simulation again until the specs are met. In **figure 8**, where an initial combination has been tried, it is obvious that the low operating frequency associated with a rather high ESR capacitor leads to prohibitive component values without completely curing the perturbations (C_FILTER=100 nF, L_FILTER=330 µH). The solution lies in selecting a higher switching frequency, choosing a capacitor characterized by a lower ESR or implementing a multi-stage filter topology.

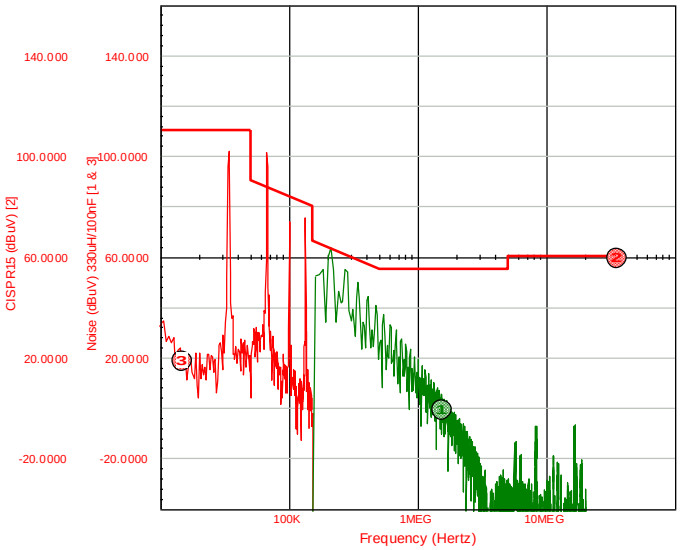


Figure 8

The parameters of the circuit can also be modified. For instance, if you remove R_6 the circuit simulates the power-on process, leading to the illumination of the tube. The currents are then much higher than in normal operation. Does your calculated filter sustain the transient without trouble ?

Displaying the standard you want

As you can see on the plots, the compliance curve is superimposed on the graphics and allows an immediate “pass or failed” evaluation. This nice feature can be accomplished with any graphical processor that is able to read SPICE compatible ASCII files and implements the copy/paste functions. You simply create a short file in which you describe the coordinates (time and amplitude) of the salient points corresponding to your compliance curve. Below is the content of an example file for the FCC part 15 class B:

.PRINT TRAN V(1)
.END

******* TRANSIENT ANALYSIS *********

TIME V(1)

450K 48
30MEG 48

The file is finally saved with the .OUT extension.

Comparison between simulated and real measured plots

The EMI tests were performed on a 32-W ballast at the Schneider Electric EMC facility in Grenoble, France. The heart of the ballast was an IR2155 operating at 33 kHz, including two 0.47 µF (C_2) capacitors wired in a half bridge configuration. There was no correcting filter at the input. We used a Rhode & Schwarz ESH3 measuring receiver. The measurement was started after a one-hour warm-up to ensure a stable operating point. **Figure 9** depicts the results, which can be compared to the simulated plot of **figure 7b**. The amplitude discrepancies between the two graphs can be explained. First, it is difficult to exactly match the real and simulated operating points, especially with a fluorescent tube as the load. Secondly, the filtering capacitor model does not account for capacity and ESR variations versus frequency and bias voltage. Lastly, the high frequency noise generated by the diodes was not incorporated into the simulations.

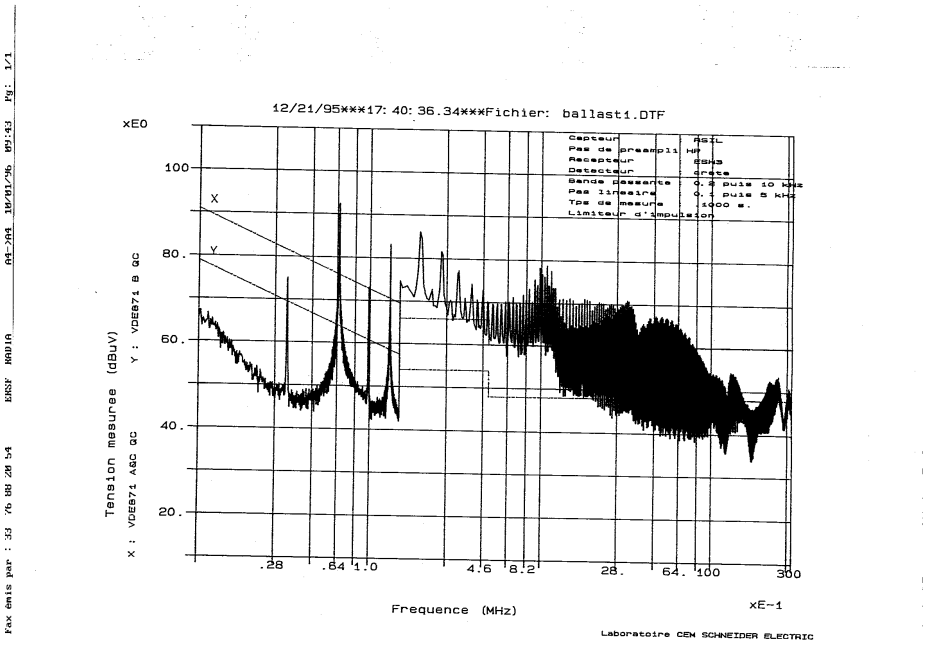


Figure 9

Input filter instabilities

The purpose of a closed loop power supply is to maintain the output power at a steady-state level. In other words, if the line voltage goes up, the input current diminishes in order to keep the power transfer constant. From the input side, this behavior can be modeled as a black box exhibiting a negative resistance. In an excited *LC* filter, the amplitude of the ringing oscillation is associated with an exponential term. The negative real part of the exponent describes the decay introduced by the ohmic losses of the coil. If by some means, the ohmic losses are perfectly compensated, the real part of the exponent would be nullified and the oscillation would never end. In our case, inserting an *LC* filter

between the mains and the SMPS can lead to instabilities if some precautions are not taken at the design stage.

A complete filter design accounts for both the filter output impedance, Z_o, and the converter input impedance, Z_{in}. To avoid instabilities, the design must fulfill the criterion: $|Z_o| << |Z_{in}|$. In this paper, we have concentrated our study on the EMI point of view. However, for those interested in simulating the complete structure including the SMPS and its filter, you can find an in-depth description in "SMPS simulation with SPICE3", recently written by Steven SANDLER (76624.1554@compuserve.com) from Analytical Engineering Services (Chandler, AZ). Reading the book written by Dr Vincent BELLO (DrVGB@AOL.COM) is also relevant for people involved in SMPS SPICE simulations.

Conclusion

This article has presented one way to predict parasitic interferences produced by electronic equipment when simulating its exact current signature. The original model can be improved by adding all the parasitic reactances and capacitances across the elements of the line filter. Unfortunately, the common mode noise cannot be easily predicted since it depends upon capacitive links induced by the overall layout and the positioning of the components on the PCB.

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