Design procedure for a PFC operated in borderline conduction mode (BCM)

$\eta := 90\%$ $P_{out} := 180W$ $F_{sw\_min} := 30kHz$

$V_{acLL} := 195V$ $V_{acHL} := 265V$ $F_{line} := 50Hz$

$V_{out} := 385V$ $V_{out\_max} := 430V$

$\delta_V := 10\%$ allowed 100-Hz output ripple

$r_{DS\_on} := 0.2\Omega$ MOSFET rDS(on) @ Tj = 100 °C

---------- NCP1608 parameter ----------

$V_{Ct} := 4.775V$ $I_{Ct} := 297\mu A$ $I_{OVP} := 10\mu A$ $V_{LIM} := 0.5V$

$$I_{L\_peak} := \frac{2\cdot\sqrt{2}\cdot P_{out}}{\eta\cdot V_{acLL}} = 2.901\,A$$

$$I_{L\_rms} := \frac{I_{L\_peak}}{\sqrt{6}} = 1.184\,A$$

$$L_1 := \frac{\eta\cdot V_{acLL}^{2}\cdot\left(\frac{V_{out}}{\sqrt{2}} - V_{acLL}\right)}{\sqrt{2}\cdot V_{out}\cdot P_{out}\cdot F_{sw\_min}} = 899.006\,\mu H$$

Inductor parameters
Choose min frequency

$$t_{on\_max} := \frac{2\cdot P_{out}\cdot L_1}{\eta\cdot V_{acLL}^{2}} = 9.457\,\mu s$$

This is a constant t_{on} PFC

$$C_t := \frac{2\cdot P_{out}\cdot L_1\cdot I_{Ct}}{\eta\cdot V_{acLL}^{2}\cdot V_{Ct}} = 588.216\,pF$$

This is the timing capacitor

$$Ratio := \frac{V_{out} - \sqrt{2}\cdot V_{acHL}}{2.3V} = 4.449$$

Turns ratio between inductor and ZCD winding. Smaller than Ratio.

$$R_{FB1} := \frac{V_{out\_max} - V_{out}}{I_{OVP}} = 4.5\times 10^{6}\,\Omega$$

The part includes an OVP triggered by an overcurrent

$$R_{EQ} := \frac{2.5V\cdot R_{FB1}}{V_{out} - 2.5V} = 29.412\,k\Omega$$

$$R_{FB2} := \frac{R_{EQ}\cdot R_{FB}}{R_{FB} - R_{EQ}} = 78.595\,k\Omega$$

Low-side resistance value

This corresponds to a bias current of: $\frac{V_{out} - V_{ref}}{R_{FB1}} = 85\,\mu A$

Pass this value to macro (I_{bias})

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$$R_{ZCD} := \frac{\sqrt{2}\cdot V_{acHL}}{I_{CL\_NEG}}\cdot\frac{1}{Ratio} = 33.692\,k\Omega$$ Min value for the RCD resistance

$$V_{out\_UV} := \frac{R_{FB1} + R_{EQ}}{R_{EQ}}\cdot 300mV = 46.2\,V$$ Undervoltage detection

---------- MOSFET transistor rms current ----------

$$I_{D\_rms} := \frac{2\cdot P_{out}}{\sqrt{3}\cdot\eta\cdot V_{acLL}}\cdot\sqrt{1 - \frac{8\cdot\sqrt{2}\cdot V_{acLL}}{3\cdot\pi\cdot V_{out}}} = 0.741\,A$$

$$P_{cond} := I_{D\_rms}^{2}\cdot r_{DS\_on} = 0.11\,W$$

$C_{oss} := 27.5pF$ Coss capacitance measured at 100 V

$$P_{SW} := \frac{2}{3}\cdot C_{oss}\cdot\sqrt{25}\cdot\left(V_{out}\right)^{2}\cdot F_{sw\_min} = 0.408\,W$$ approximated switching losses

---------- Sense resistance ----------

$$R_{sense} := \frac{V_{LIM}}{I_{L\_peak}} = 0.172\,\Omega$$

$$P_R := I_{D\_rms}^{2}\cdot R_{sense} = 0.095\,W$$

--------- Output capacitor design ----------

$$C_{out} := \frac{P_{out}}{2\cdot\pi\cdot F_{line}\cdot V_{out}^{2}\cdot\delta_V} = 38.655\,\mu F$$

$$I_{C\_rms} := \sqrt{\frac{32\cdot\sqrt{2}\cdot P_{out}^{2}}{9\cdot\pi\cdot V_{acLL}\cdot V_{out}\cdot\eta^{2}} - \left(\frac{P_{out}}{V_{out}}\right)^{2}} = 0.796\,A$$ Low-frequency ripple current

Chose: $C_{out} := 82\mu F$ $V_{min} := 330V$ Minimum acceptable output voltage

$$t_{hold\_up} := \frac{C_{out}\cdot\left(V_{out}^{2} - V_{min}^{2}\right)}{2\cdot P_{out}} = 8.957\,ms$$ The time it takes at Pout for Vout to drop from Vout to Vmin

- BCM Power factor correction - VM - ac.asc
- BCM Power factor correction - VM - fixed load.asc
- BCM Power factor correction - VM - load step.asc

Run BCM *PFC – VM – ac* to extract the ac response. Pass the calculated parameters to the macros.

This is a BCM PFC averaged model.
Operating parameters are from NCP1608

1. Select lowest Vin and max load
2. Plot V(out)/V(err)
3. Extract mag and phase at crossover (e.g. 5 Hz in low line)
4. Feed the macro with what you've extracted
5. Run another ac analysis, plot V(out)/V(in)
6. Check crossver and margins are ok
7. Increase Vin to max and check margins again

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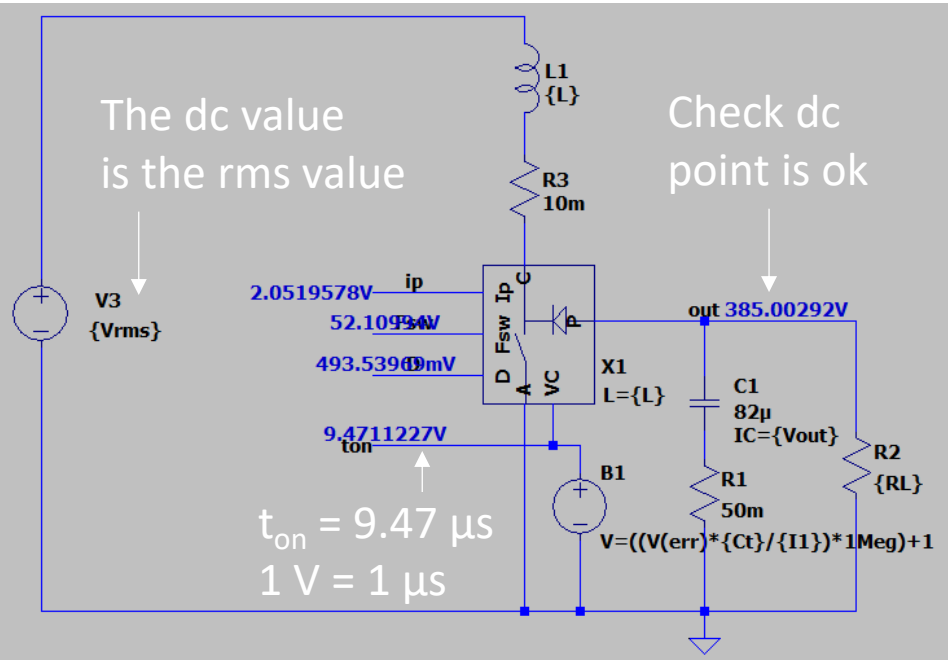
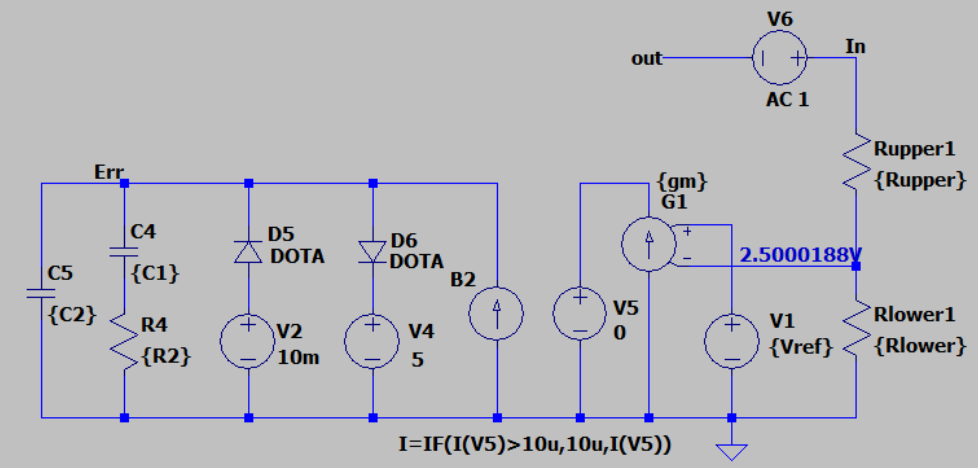
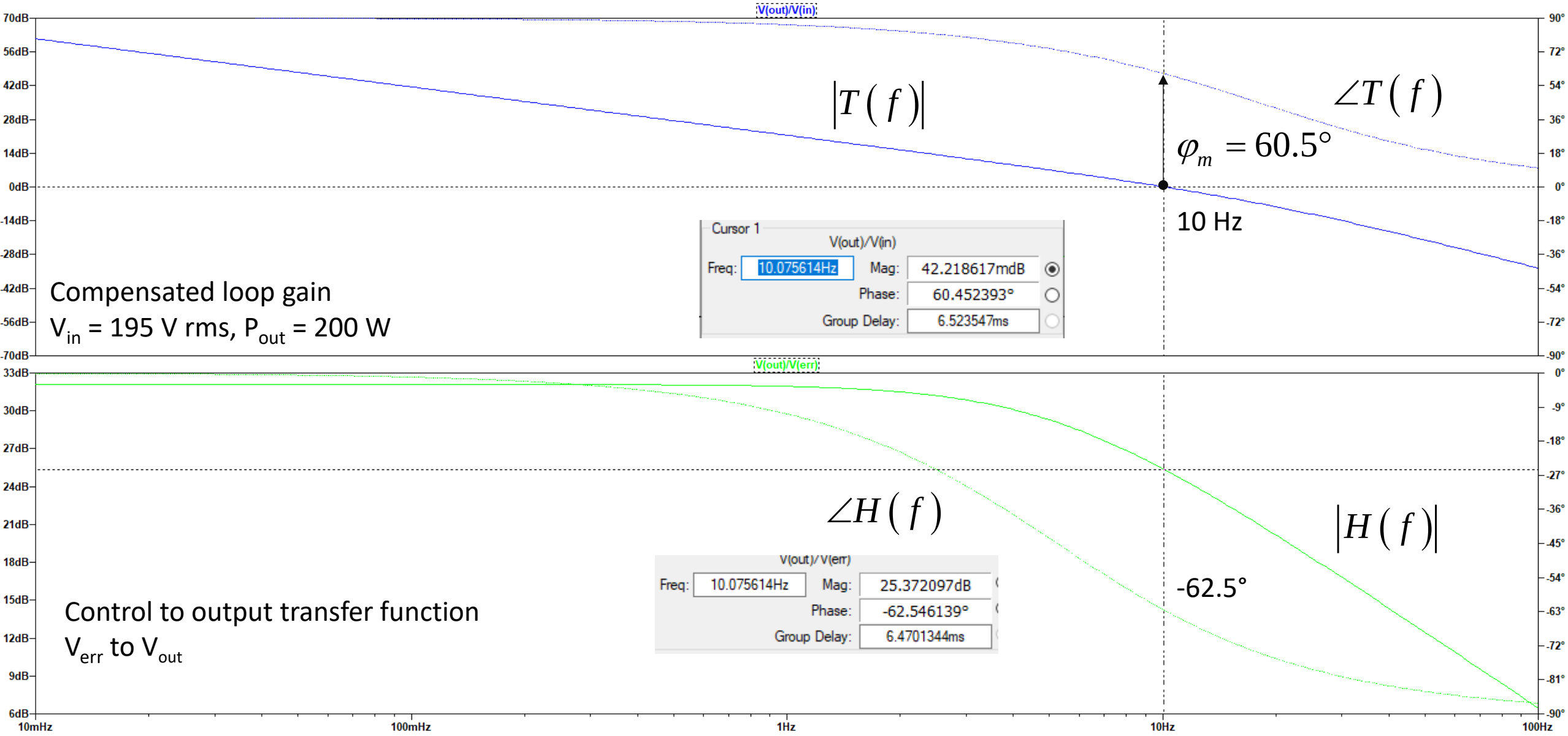
```
.model DPFC D TT=100n Rs=10m Cjo=50p N=0.6
.model DOTA D tt=100n Rs=10m N=100m
*
.param Vrms=195
.param Pout=200
.param Vout=385
.param RL={Vout**2/Pout}
.param L=900u
.param Ct=588p
.param I1=297u

.ac dec 100 10m 100

.options abstol=1u vntol=1m reltol=0.01 gmin=100p
+method=gear
```



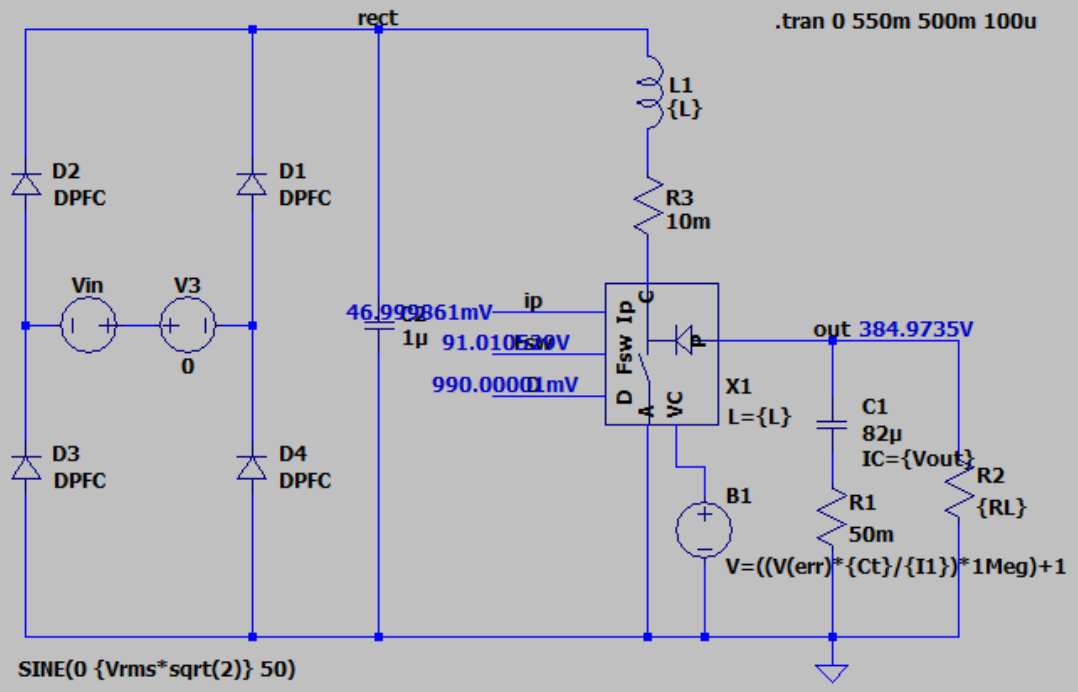

```
*
.param Gfc=25.3 ; magnitude at crossover *
.param PS=-63 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fc=10 ; targeted crossover *
.param PM=60 ; choose phase margin at crossover *
*
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Ibias=250u
.param Vref=2.5
*
* Do not edit the below lines *
*
.param gm=100u ; transconductance in Siemens *
.param Rlower={Vref/Ibias}
.param Rupper={(Vout-Vref)/Ibias}
.param boost={PM-PS-90}
.param G={10**(-Gfc/20)}
.param kf={tan((boost/2+45)*pi/180)}
.param fp={fc*kf}
.param fz={fc/kf}
.param a={sqrt((fc**2/fp**2)+1)}
.param b={sqrt((fz**2/fc**2)+1)}
.param R2={(a/b)*(fp*G)*(Rlower+Rupper)/((fp-fz)*Rlower*gm)}
.param C1={1/(2*pi*R2*fz)}
.param C2={Rlower*gm*(b/a)/(2*pi*fp*G*(Rlower+Rupper))}
*
```

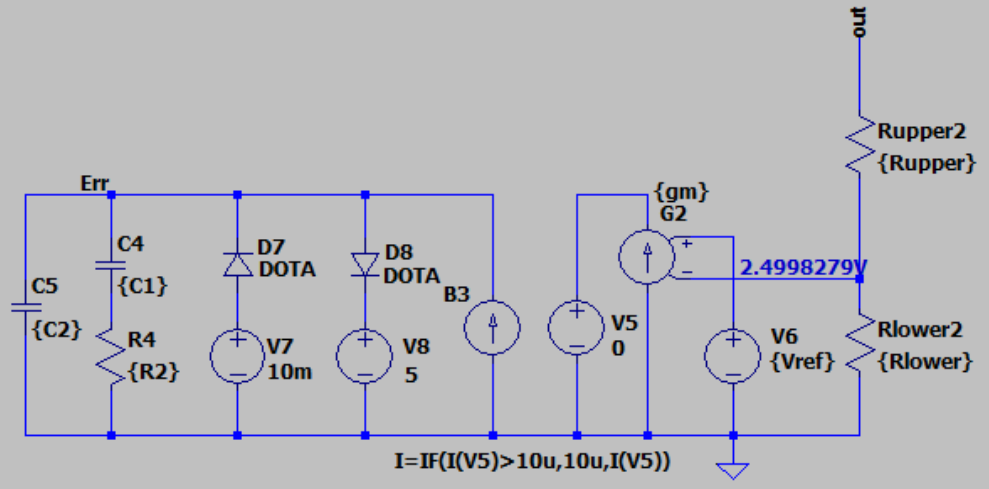


From the simulation, you can plot the power stage response H(s) and compensated the loop gain.



Reproduce the adopted values for the power stage and run BCM *PFC – VM – fixed load* to extract the operating parameters.

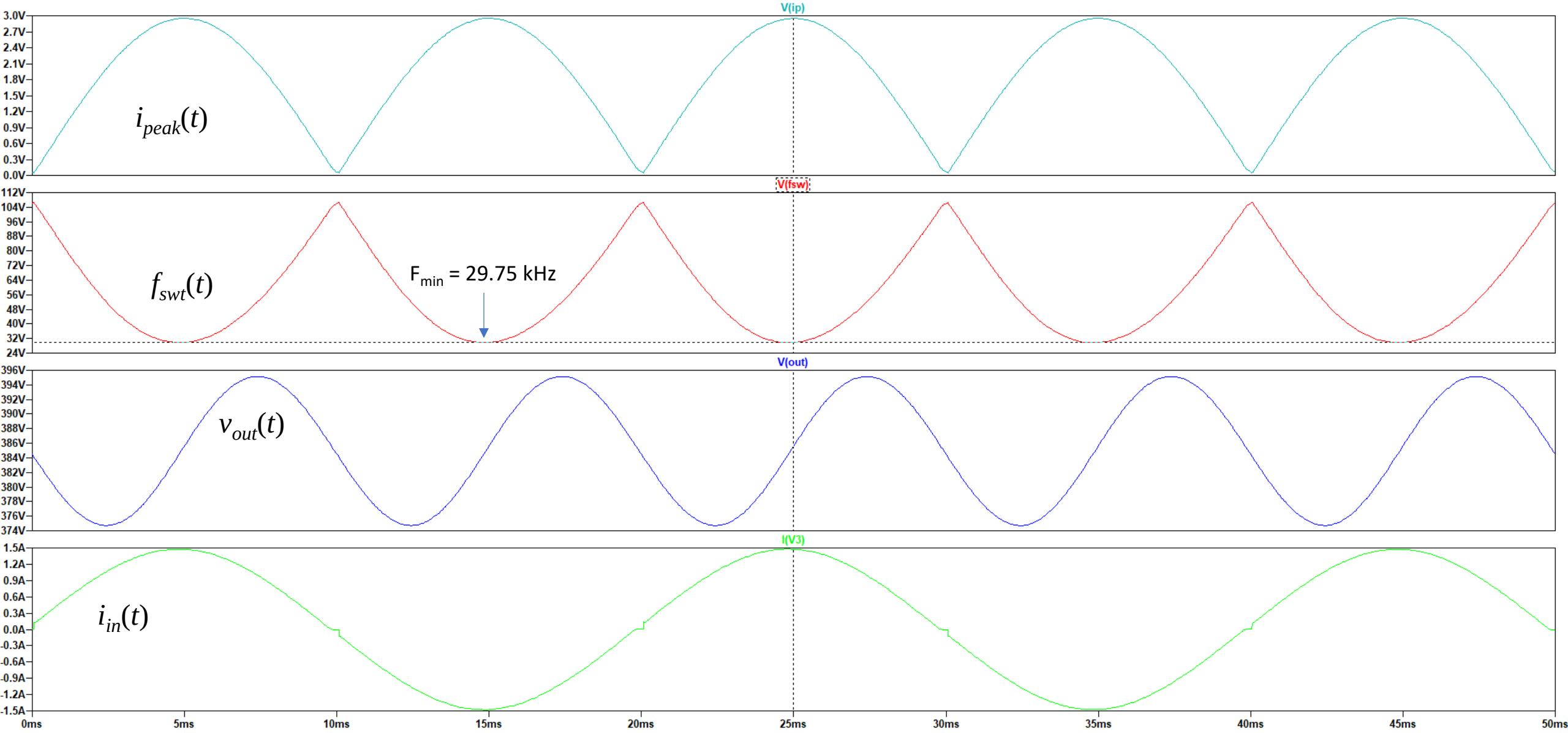




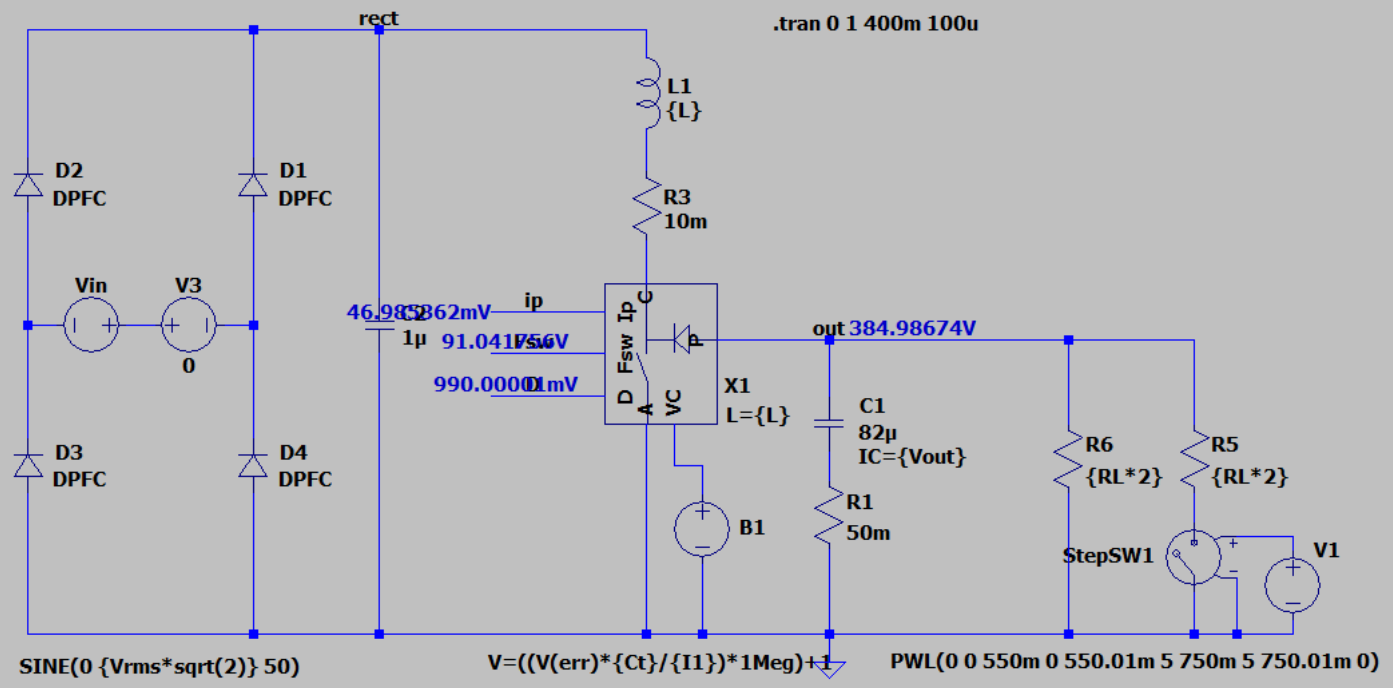

```
.model DPFC D TT=100n Rs=10m Cjo=50p N=0.6
.model DOTA D tt=100n Rs=10m N=100m
*
.param Vrms=195
.param Pout=200
.param Vout=385
.param RL={Vout**2/Pout}
.param L=900u
.param Ct=588p
.param I1=297u
*
.param Gfc=25.3 ; magnitude at crossover *
.param PS=-62 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fc=10 ; targeted crossover *
.param PM=60 ; choose phase margin at crossover *
*
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Ibias=250u
.param Vref=2.5
*
* Do not edit the below lines *
*
.param gm=100u ; transconductance in Siemens *
.param Rlower={Vref/Ibias}
.param Rupper={(Vout-Vref)/Ibias}
.param boost={PM-PS-90}
.param G={10**(-Gfc/20)}
.param kf={tan((boost/2+45)*pi/180)}
.param fp={fc*kf}
.param fz={fc/kf}
.param a={sqrt((fc**2/fp**2)+1)}
.param b={sqrt((fz**2/fc**2)+1)}
.param R2={(a/b)*(fp*G)*(Rlower+Rupper)/((fp-fz)*Rlower*gm)}
.param C1={1/(2*pi*R2*fz)}
.param C2={Rlower*gm*(b/a)/(2*pi*fp*G*(Rlower+Rupper))}
*

.options abstol=1u vntol=1m reltol=0.01 gmin=100p
+method=gear
```

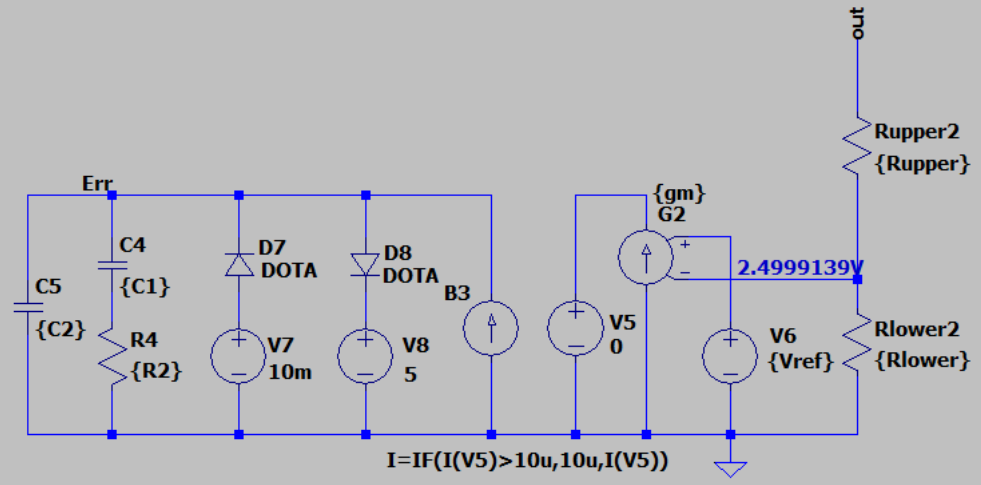
Values coming from ac analysis

```
*
.param Gfc=25.3 ; magnitude at crossover *
.param PS=-63 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fc=10 ; targeted crossover *
.param PM=60 ; choose phase margin at crossover *
*
```


V(ip)
3.0V
2.7V
2.4V
2.1V
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
$i_{peak}(t)$
V(fsw)
112V
104V
96V
88V
80V
72V
64V
56V
48V
40V
32V
24V
$f_{swt}(t)$
F_{min} = 29.75 kHz
V(out)
396V
394V
392V
390V
388V
386V
384V
382V
380V
378V
376V
374V
$v_{out}(t)$
I(V3)
1.5A
1.2A
0.9A
0.6A
0.3A
0.0A
-0.3A
-0.6A
-0.9A
-1.2A
-1.5A
$i_{in}(t)$
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms

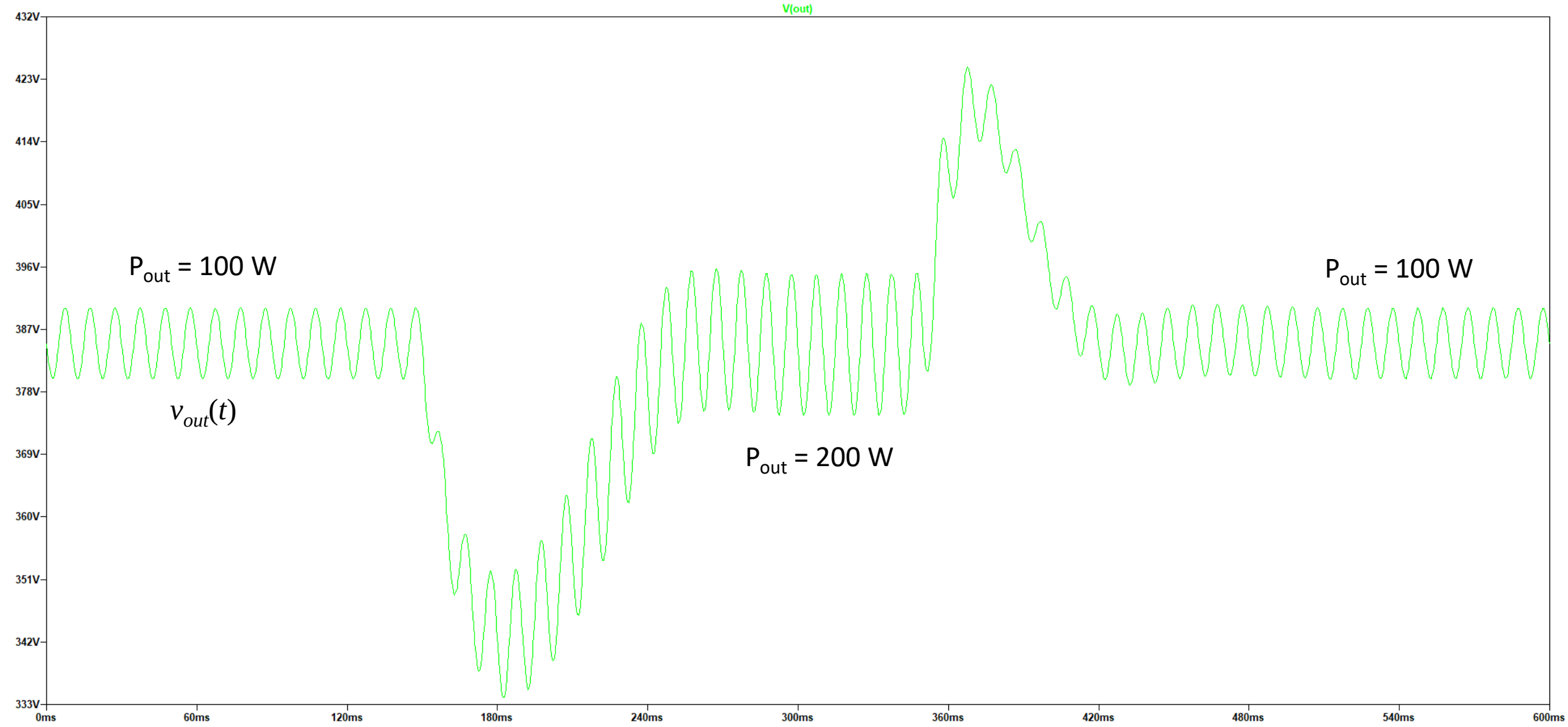
Now you can run BCM *PFC – VM – step load* to check stability is ok and undershoots/overshoots are acceptable.



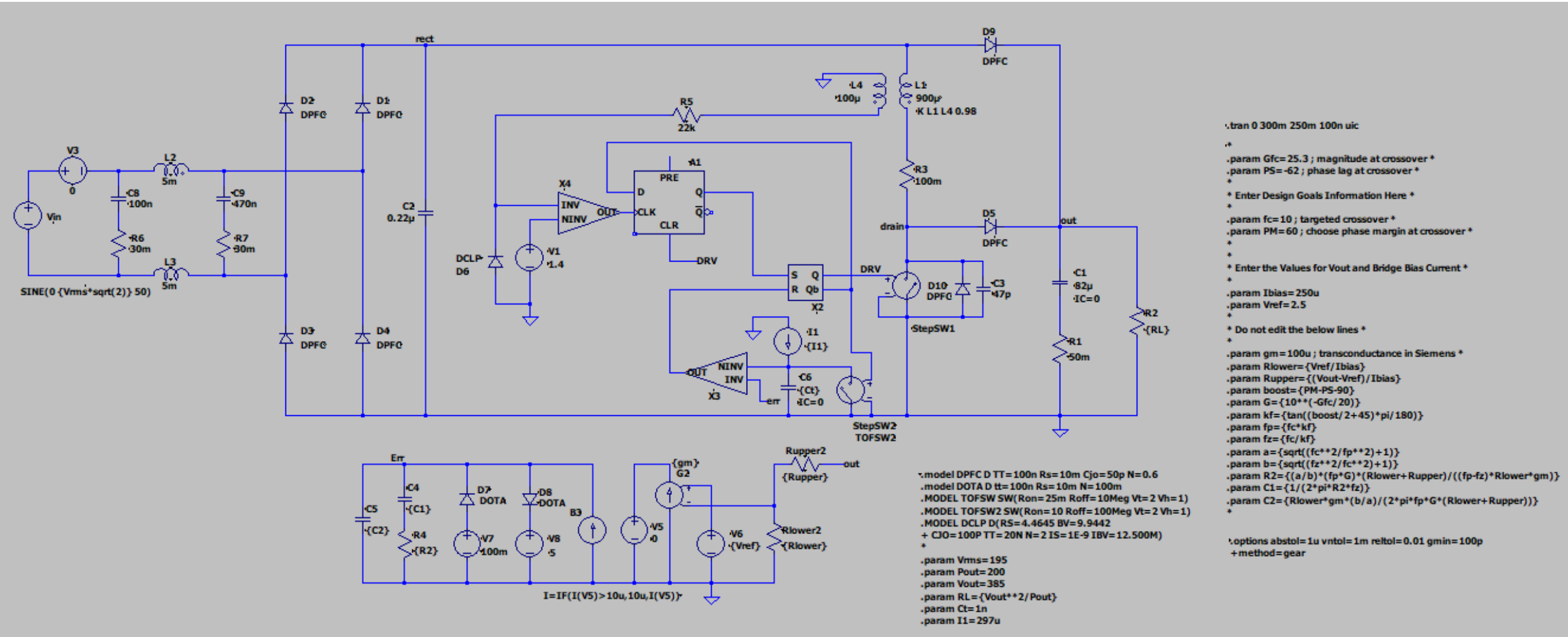



```
.model DPFC D TT=100n Rs=10m Cjo=50p N=0.6
.model DOTA D tt=100n Rs=10m N=100m
.MODEL TOFSW SW(Ron=25m Roff=10Meg Vt=2 Vh=1)
*
.param Vrms=195
.param Pout=200
.param Vout=385
.param RL={Vout**2/Pout}
.param L=900u
.param Ct=588p
*param I1=297u
.param Gfc=25.3 ; magnitude at crossover *
.param PS=-63 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fc=10 ; targeted crossover *
.param PM=60 ; choose phase margin at crossover *
*
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Ibias=250u
.param Vref=2.5
*
* Do not edit the below lines *
*
.param gm=100u ; transconductance in Siemens *
.param Rlower={Vref/Ibias}
.param Rupper={(Vout-Vref)/Ibias}
.param boost={PM-PS-90}
.param G={10**(-Gfc/20)}
.param kf={tan((boost/2+45)*pi/180)}
.param fp={fc*kf}
.param fz={fc/kf}
.param a={sqrt((fc**2/fp**2)+1)}
.param b={sqrt((fz**2/fc**2)+1)}
.param R2={(a/b)*(fp*G)*(Rlower+Rupper)/((fp-fz)*Rlower*gm)}
.param C1={1/(2*pi*R2*fz)}
.param C2={Rlower*gm*(b/a)/(2*pi*fp*G*(Rlower+Rupper))}
*


.options abstol=1u vntol=1m reltol=0.01 gmin=100p
+method=gear
```

The power is stepped from 50 to 100% (100 to 200 W). If the undershoot is too deep, you can increase the output capacitance (re-run ac analysis) or push crossover a little. Crossover changes with the ratio V_{inHL}/V_{inLL} square. The max f_c should around 20-30 Hz at V_{inHL} for best input current distortion figures.



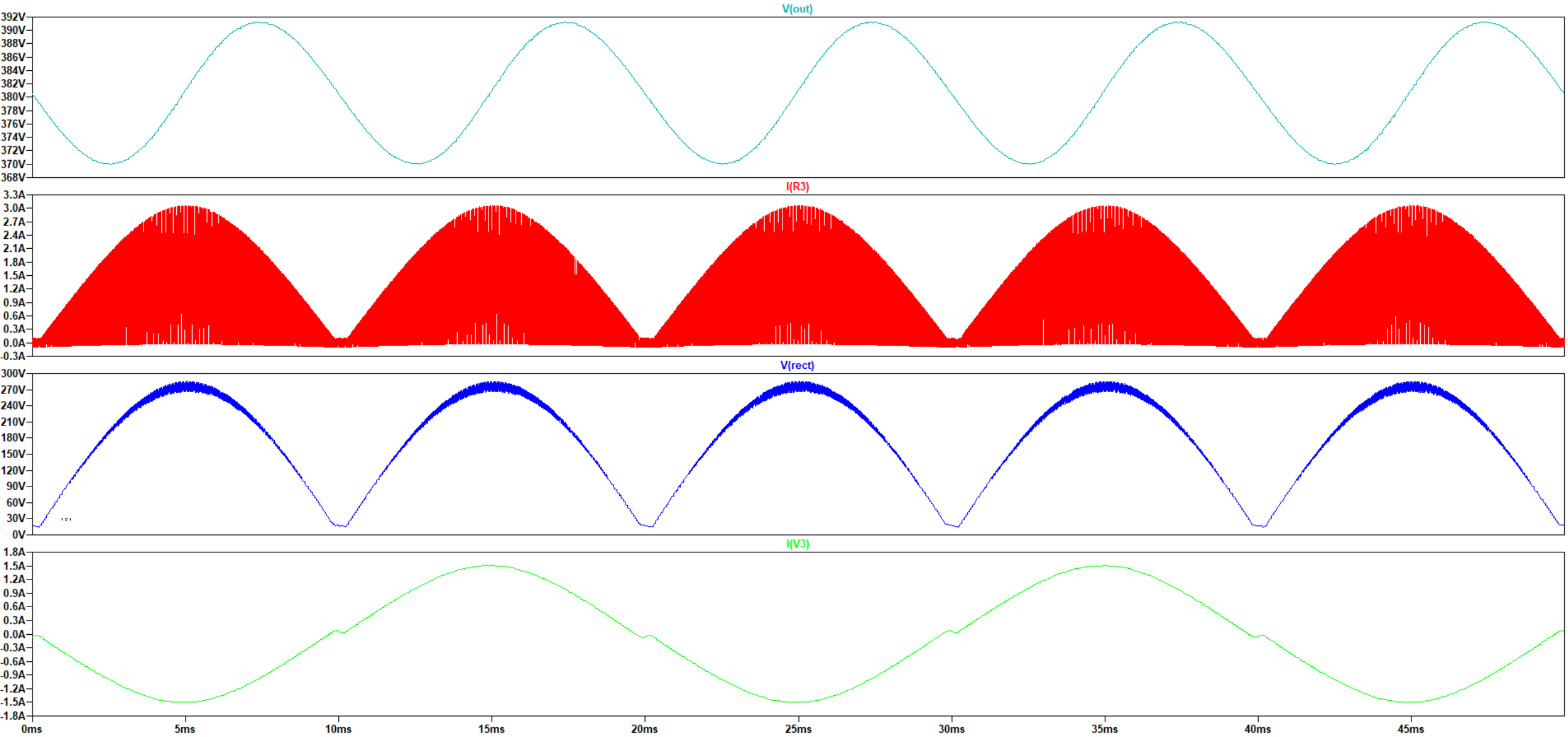
This is now the cycle-by-cycle simulation and the error amplifier is compensated from the averaged model. The simulation time is acceptable for a few line cycles. Beyond, the amount of data can become problematic and the display of a given waveform may take some time.




```
.tran 0 300m 250m 100n uic
*
.param Gfc=25.3 ; magnitude at crossover *
.param PS=-62 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fc=10 ; targeted crossover *
.param PM=60 ; choose phase margin at crossover *
*
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Ibias=250u
.param Vref=2.5
*
* Do not edit the below lines *
*
.param gm=100u ; transconductance in Siemens *
.param Rlower={Vref/Ibias}
.param Rupper={(Vout-Vref)/Ibias}
.param boost={PM-PS-90}
.param G={10**(-Gfc/20)}
.param kf={tan((boost/2+45)*pi/180)}
.param fp={fc*kf}
.param fz={fc/kf}
.param a={sqrt((fc**2/fp**2)+1)}
.param b={sqrt((fz**2/fc**2)+1)}
.param R2={(a/b)*(fp*G)*(Rlower+Rupper)/((fp-fz)*Rlower*gm)}
.param C1={1/(2*pi*R2*fz)}
.param C2={Rlower*gm*(b/a)/(2*pi*fp*G*(Rlower+Rupper))}
*

.options abstol=1u vntol=1m reltol=0.01 gmin=100p
 +method=gear
```

```
.model DPFC D TT=100n Rs=10m Cjo=50p N=0.6
.model DOTA D tt=100n Rs=10m N=100m
.MODEL TOFSW SW(Ron=25m Roff=10Meg Vt=2 Vh=1)
.MODEL TOFSW2 SW(Ron=10 Roff=100Meg Vt=2 Vh=1)
.MODEL DCLP D(RS=4.4645 BV=9.9442
+ CJO=100P TT=20N N=2 IS=1E-9 IBV=12.500M)
*
.param Vrms=195
.param Pout=200
.param Vout=385
.param RL={Vout**2/Pout}
.param Ct=1n
.param I1=297u
```

The waveforms are good looking, V_{in} = 195 V rms and P_{out} = 200 W.



The waveforms are good looking, V_{in} = 230 V rms and P_{out} = 200 W. The ripple is a bit strong for a 385-V output. The peak of the rectified input shall always be less than the valley voltage otherwise the PFC operations are disturbed in high-line conditions. You can either increase the output capacitance or bring the dc output to 400 V.