



**FUTURE**  
**ELECTRONICS**

A WT Microelectronics Company

# Simulating Power Factor Correction Stages in Single- and Three-Phase Networks

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# Agenda

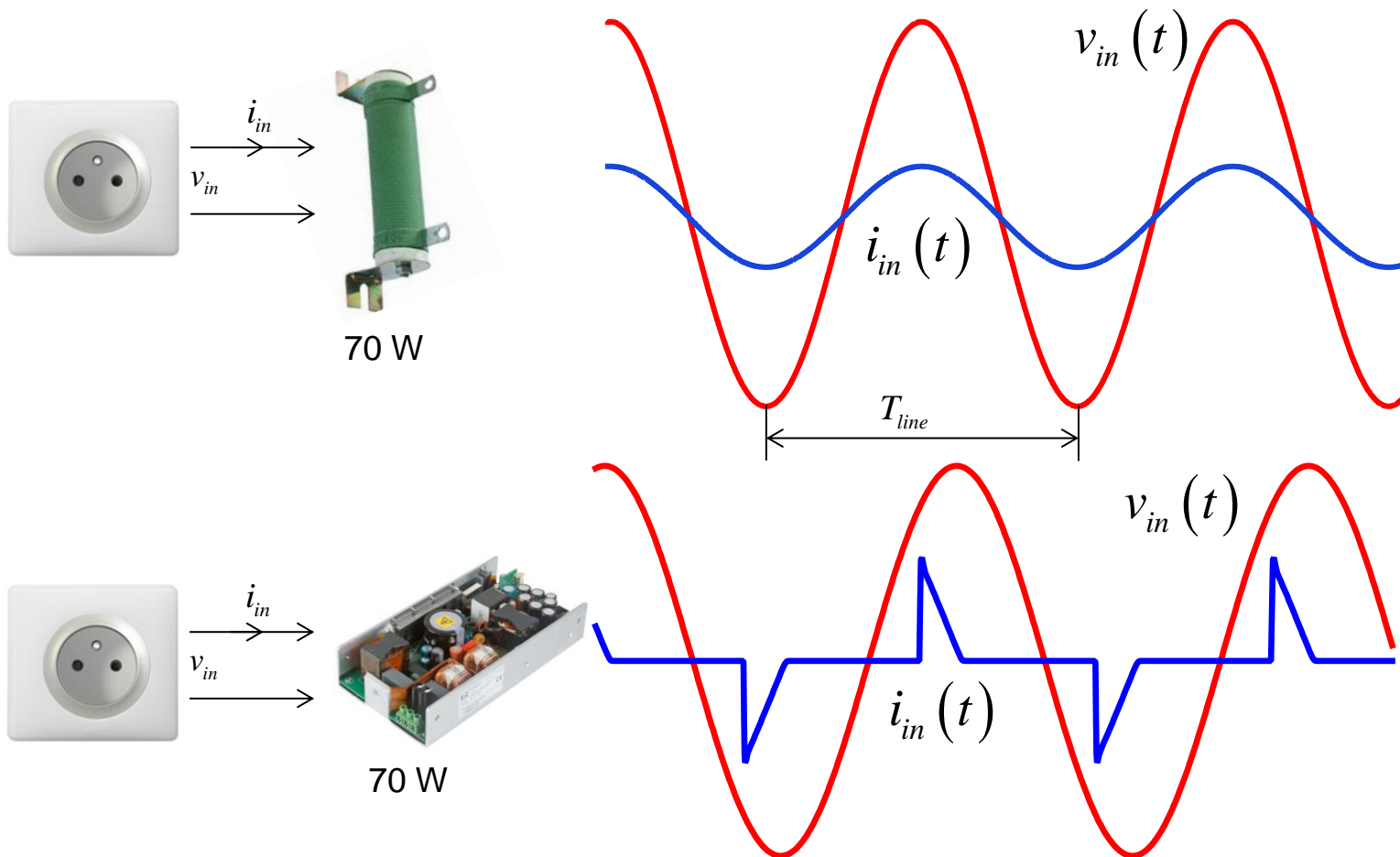
- Notions of Power Factor
- PFC Architectures
- Processing Power – Single Phase
- Processing Power – Three Phases

# Agenda

- **Notions of Power Factor**
- PFC Architectures
- Processing Power – Single Phase
- Processing Power – Three Phases

# What is Power Factor?

- The goal of any power factor correction circuit is to emulate a resistance
- The absorbed current must be sinusoidal and in phase with the input voltage



$$p_{in}(t) = i_{in}(t)v_{in}(t) = \frac{v_{in}(t)}{R}v_{in}(t)$$

$$P_{in,avg} = \frac{1}{T_{line}} \int_0^{T_{line}} p_{in}(t) \cdot dt = 70 \text{ W}$$

$$P_{in,app} = V_{in,rms} \cdot I_{in,rms} = 85 \times 823m = 70 \text{ VA}$$

$$\text{PF} = \frac{\text{active power}}{\text{apparent power}} = \frac{[\text{W}]}{[\text{V} \cdot \text{A}]} = 1$$

$$P_{in,avg} = \frac{1}{T_{line}} \int_0^{T_{line}} p_{in}(t) \cdot dt = 70 \text{ W}$$

$$P_{in,app} = V_{in,rms} \cdot I_{in,rms} = 85 \times 1.46 = 124 \text{ VA}$$

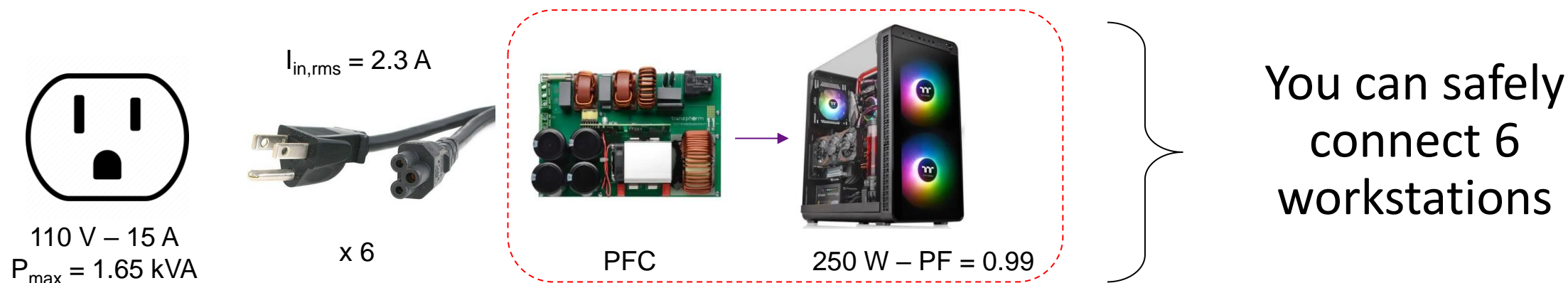
$$\text{PF} = \frac{\text{active power}}{\text{apparent power}} = \frac{[\text{W}]}{[\text{V} \cdot \text{A}]} = 0.56$$

# What is the Impact of a Low PF?

- Assume a 250-W load absorbed by an equipment from a 110-V 15-A ac outlet
- With a PF of 0.56, the current is  $250/110/0.56 \approx 4 \text{ A rms}$
- ✓ You can safely connect a maximum of 3 devices ( $15/4 = 3.75$ )

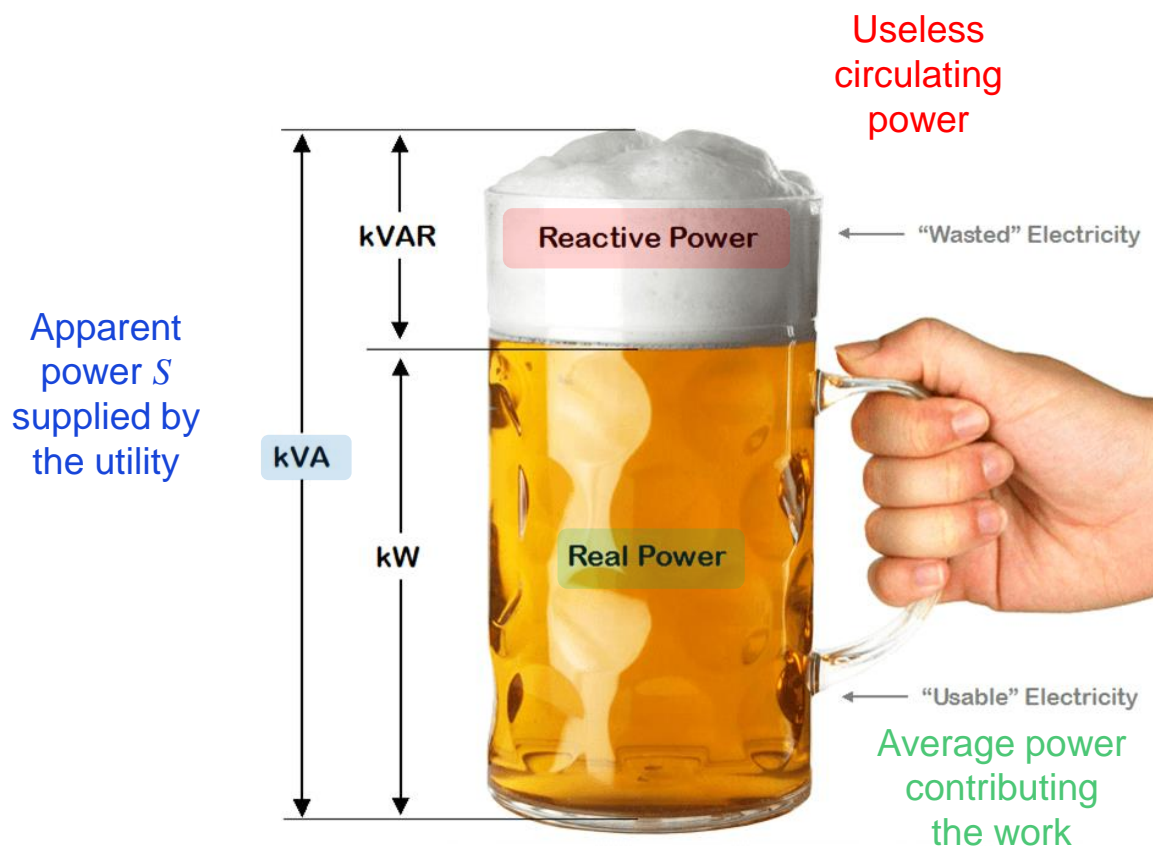


- Add a front-end power factor correction stage to bring PF close to unity



# Explaining Power Factor with Beer

- A low power factor will force the production and circulation of a higher rms current
- Electric wires can overheat and utility companies push for power factor correction
- ✓ A glass of beer with an excessive foam can help understand the issue



Over 15kW

Rates 3.0A - 3.1A y 6.x

Billed solely when reactive power exceeds 33% of the active power. It is not applied in the off-peak period (P3 of rate 3.X and P6 of rate 6.X).

$$[VA] \quad [W] \quad [VAR]$$

$$S = P + jQ$$

$$\left| \frac{P}{PF} \right| = \sqrt{P^2 + Q^2}$$

$$Q = P \sqrt{\frac{1}{PF^2} - 1}$$



If PF < 0.95

$$Q [VAR] > 33\% \cdot P [W]$$



# Power Factor and Distortion

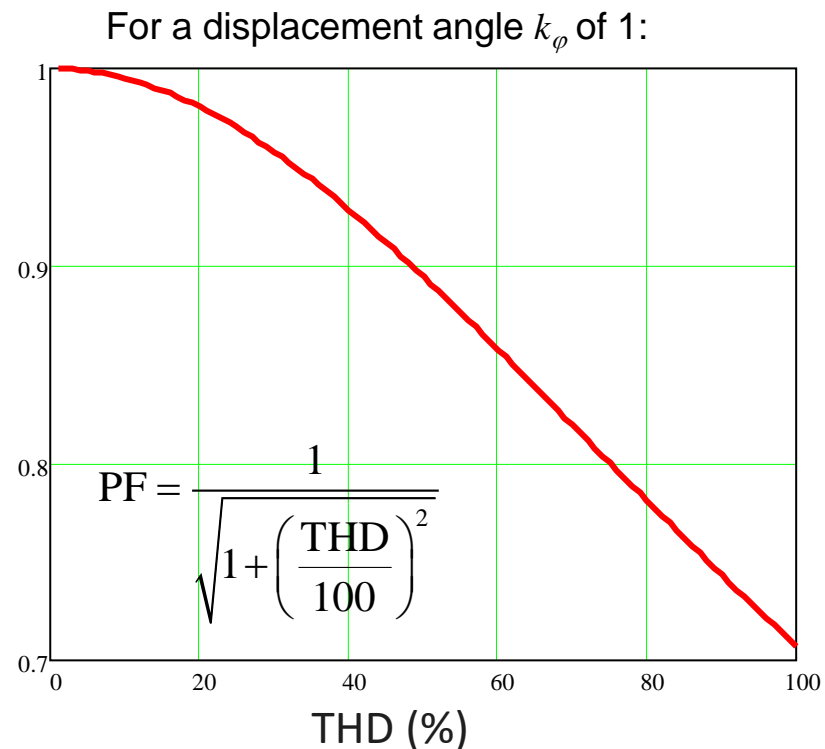
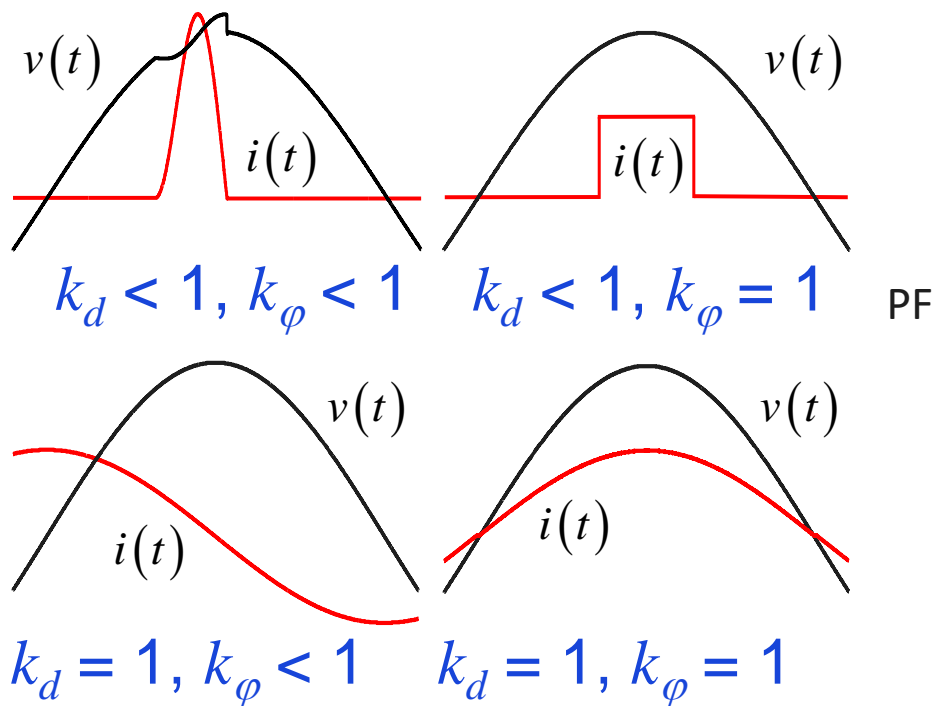
- Power factor depends on two parameters:

$$PF = \frac{I_{1,rms}}{I_{rms}} \cos \varphi = k_d k_\varphi$$

Fundamental rms current
Total rms current

✓  $k_d$  represents the distortion factor

✓  $k_\varphi$  designates the displacement angle



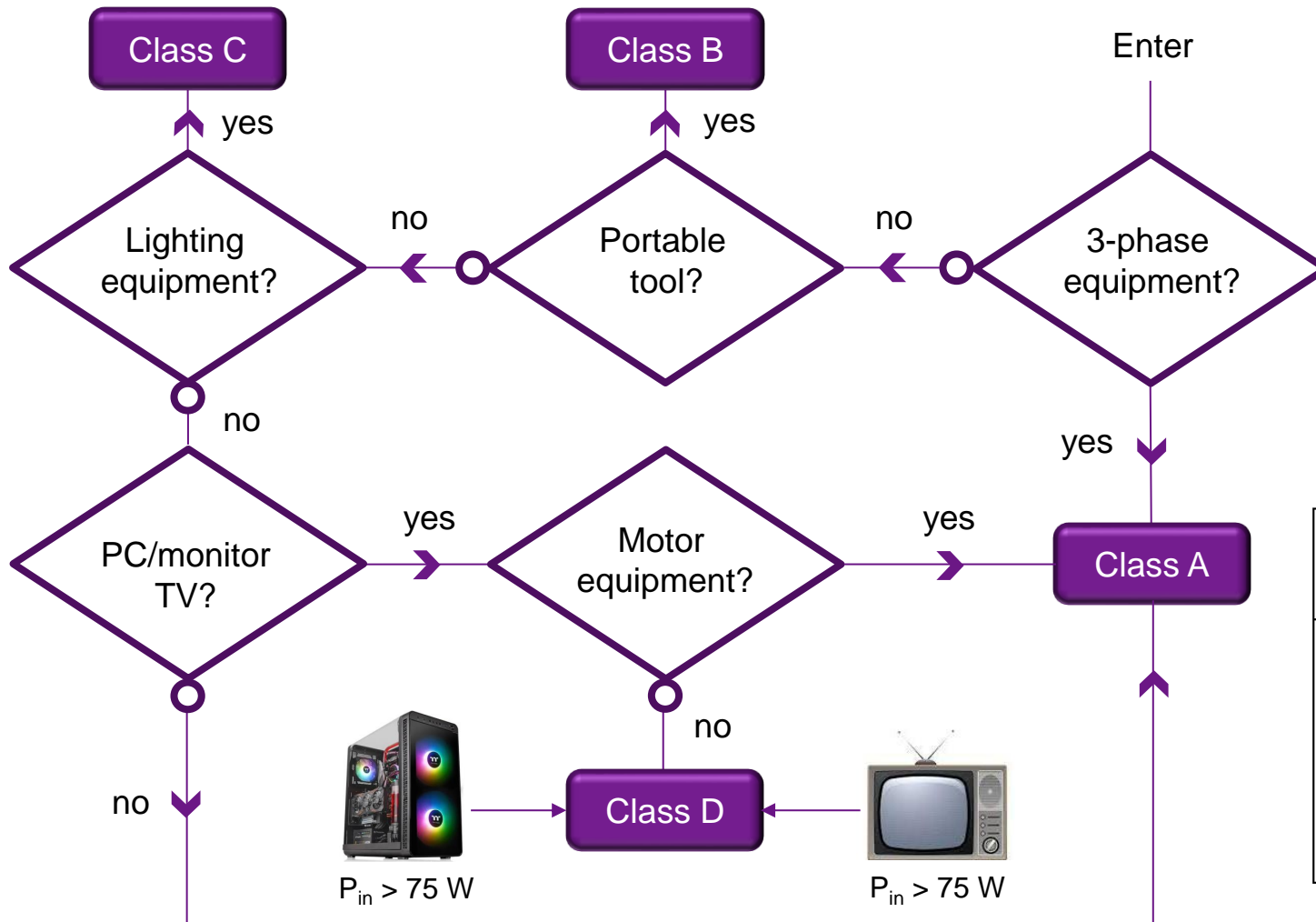
THD = 30%, PF = 0.958  
 THD = 10% PF = 0.995  
 THD = 5% PF = 0.999



Check harmonics limits according to IEC1000-3-2

# Equipment Compliance

- The standard EN61000-3-2 defines the class of equipment and associated limits



NORME  
INTERNATIONALE  
INTERNATIONAL  
STANDARD

**CEI  
IEC**  
**61000-3-2**  
Deuxième édition  
Second edition  
2000-08

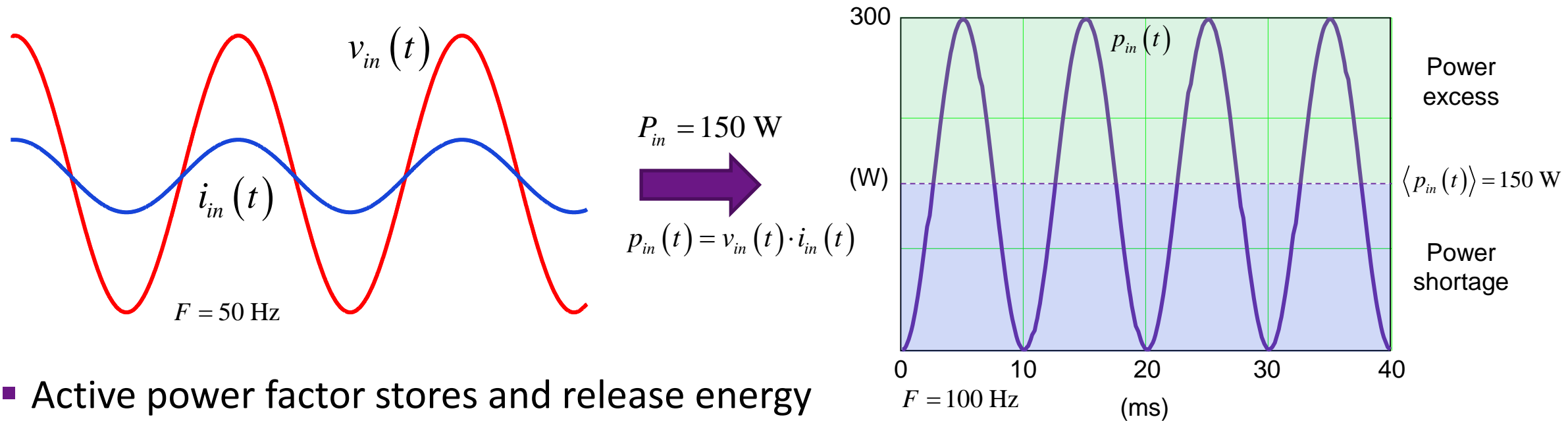


Class D limits

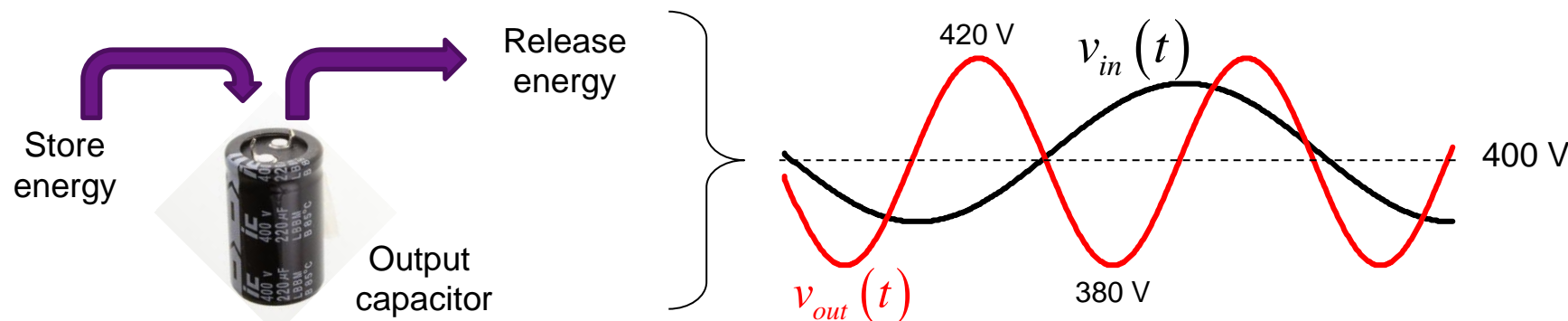
Rang harmonique	Courant harmonique maximal autorisé par watt mA/W	Courant harmonique maximal autorisé A
n		A
3	3,4	2,30
5	1,9	1,14
7	1,0	0,77
9	0,5	0,40
11	0,35	0,33
13 ≤ n ≤ 39 (harmoniques impairs seulement)	$\frac{3,85}{n}$	Voir tableau 1

# Storage Need in a Single-Phase Grid

- The goal of a PFC front-end converter is to emulate a resistive load
- The power of a single-phase ac source feeding a resistance involves a squared sinewave



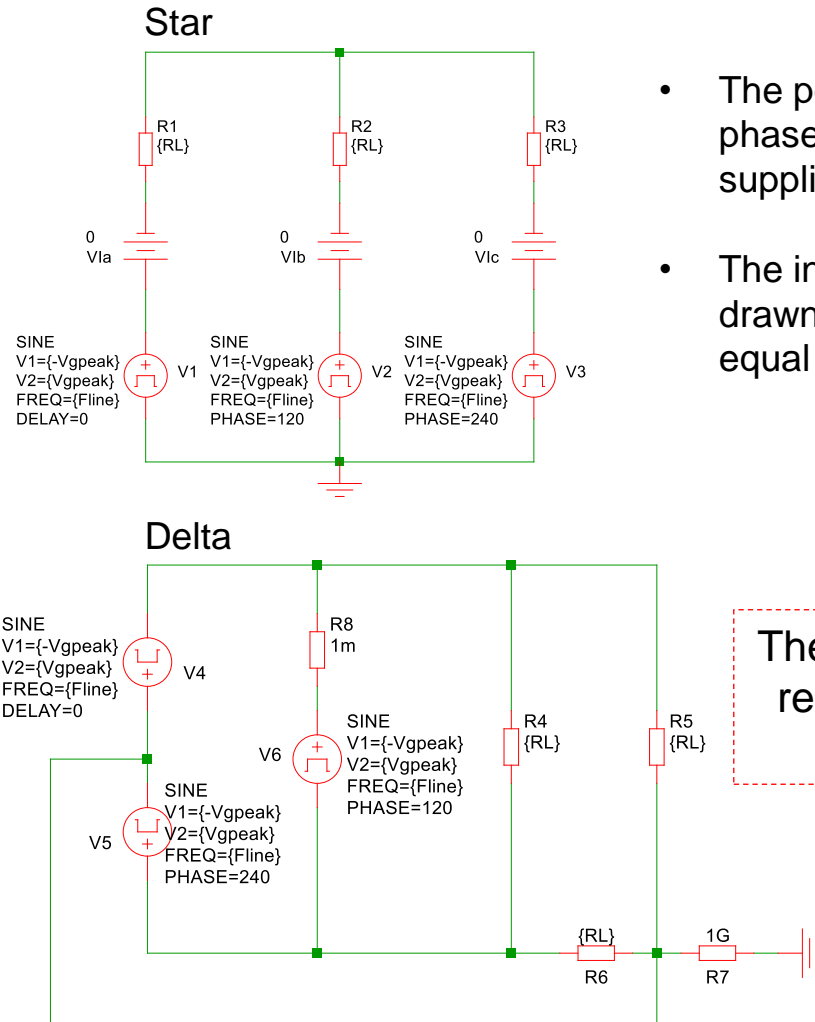
- Active power factor stores and release energy



✓ Output voltage ripple is twice the input frequency

# Instantaneous Power in a 3-Phase Grid

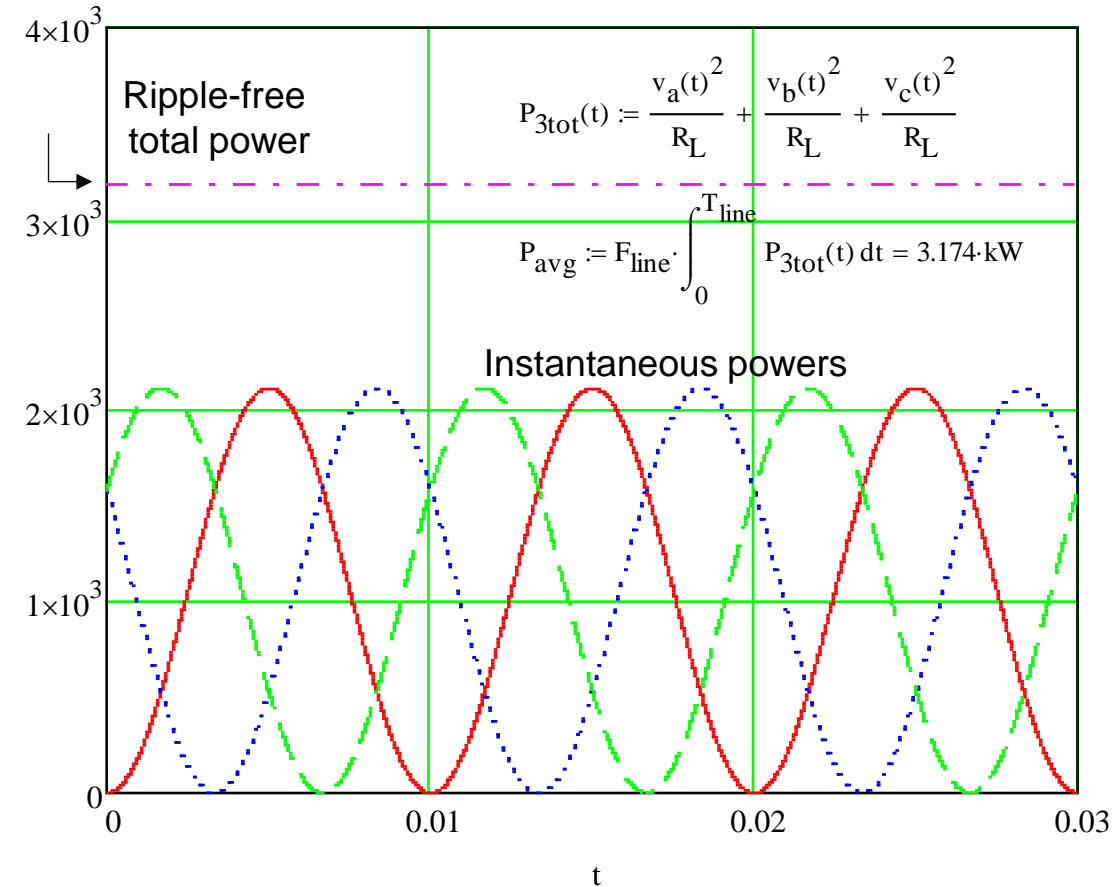
- The total power in a three-phase system is the sum of individual powers



- The power drawn from the 3-phase grid is the sum of powers supplied by phases a, b and c
- The instantaneous power drawn from the grid is a flat line equal to  $3 \times 1.058\text{k} = 3.174\text{ kW}$

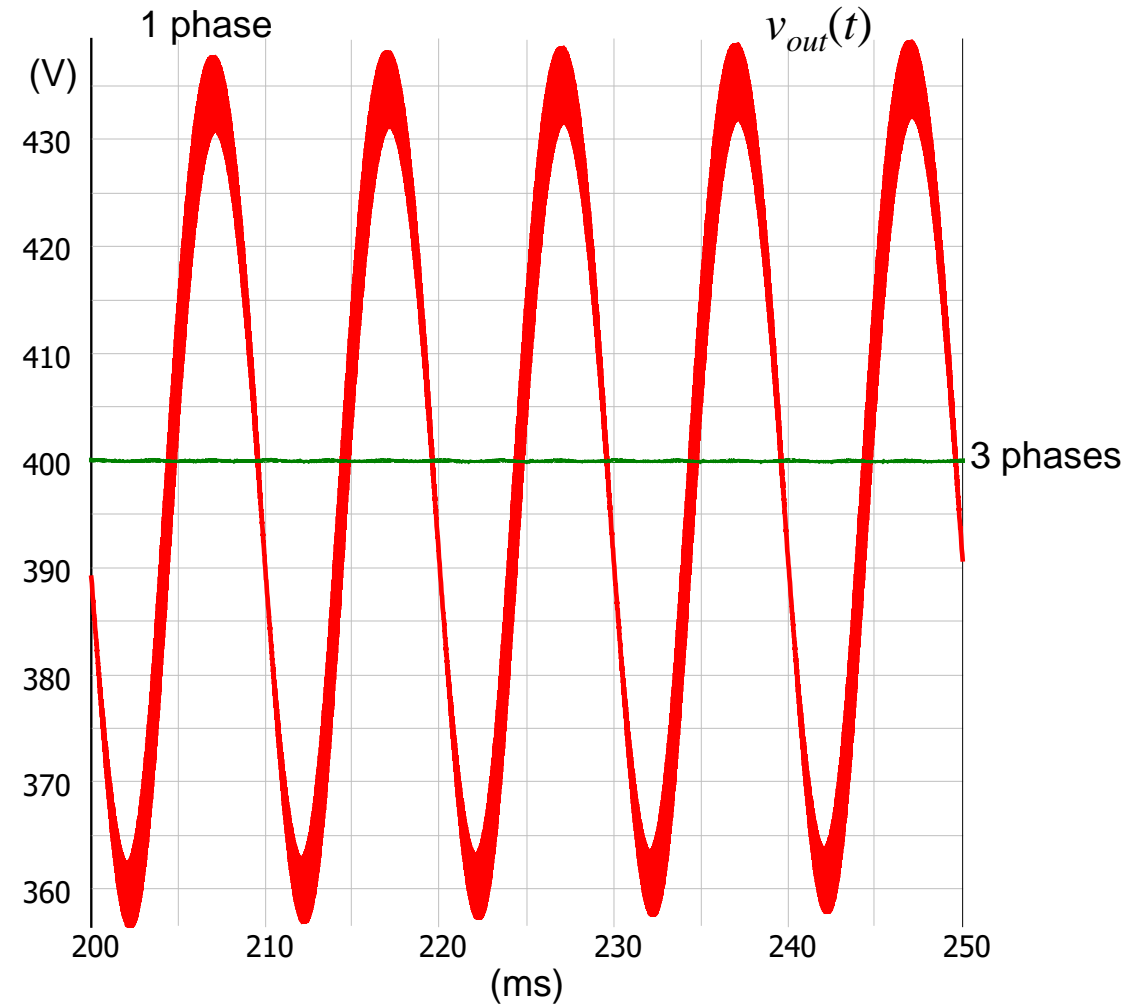
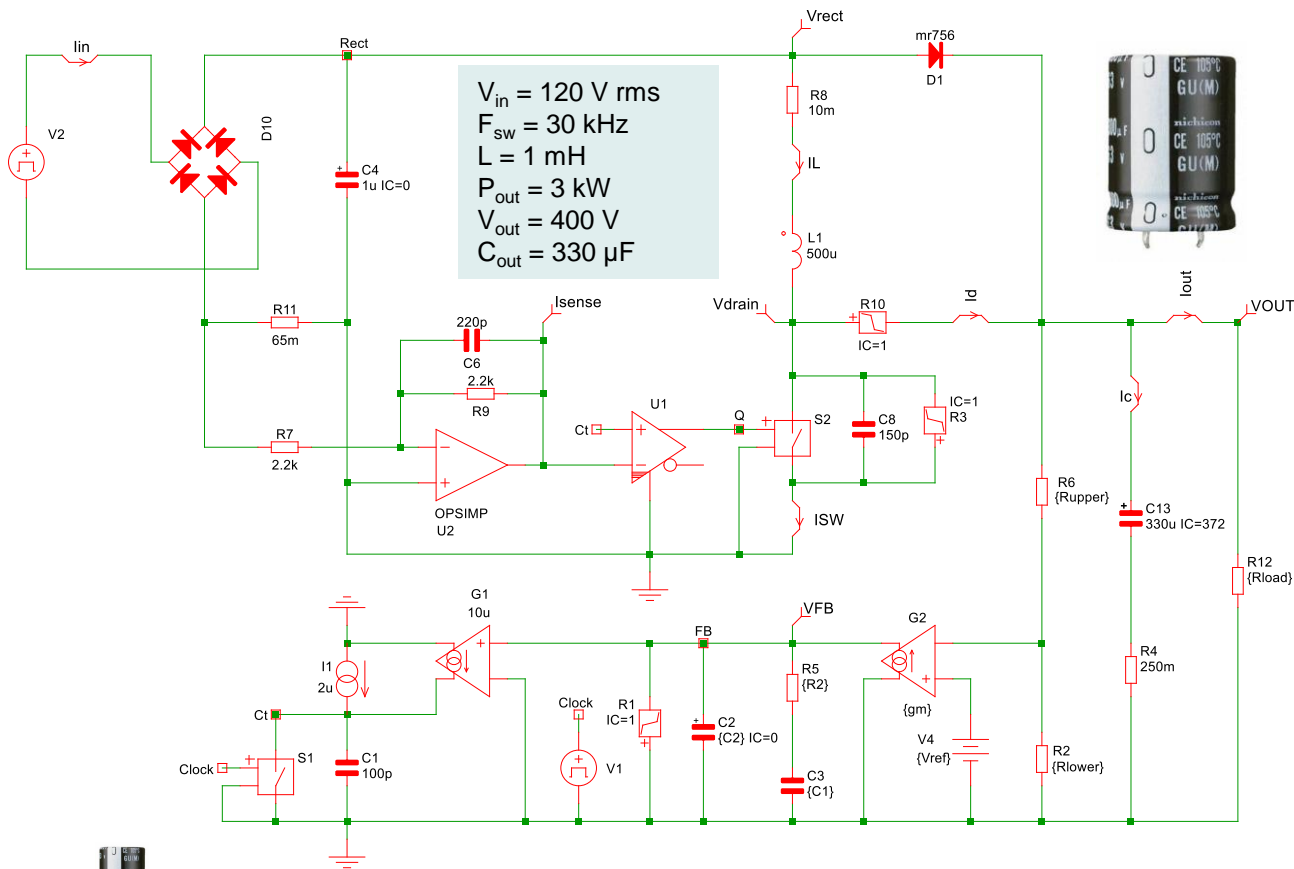


The need for storage is reduced in a 3-phase PFC



# Output Ripple in 1- and 3-Phase PFCs

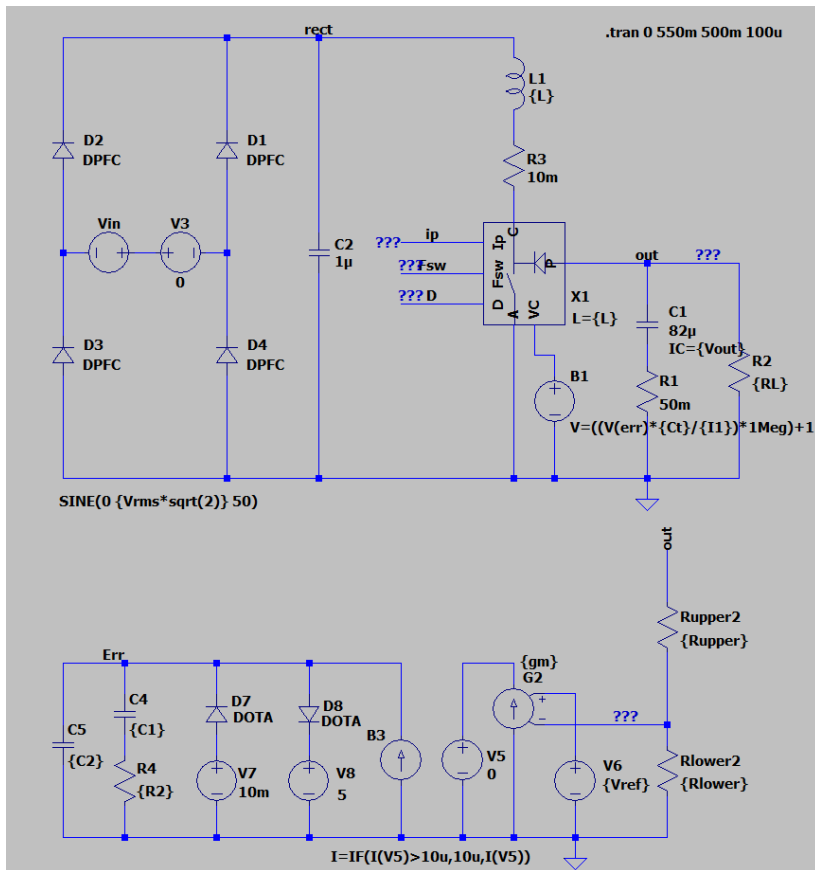
- Below is the comparison between a 3-kW PFC output ripple in a 1- or 3-phase grid



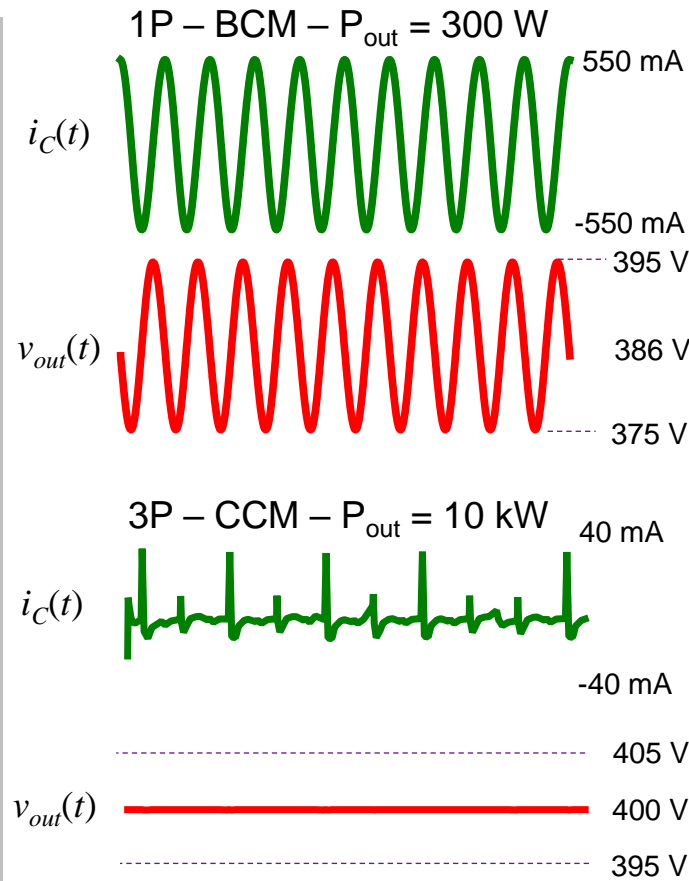
1 phase: strong low-frequency rms component  
 3 phases: no low-frequency component

# Averaged Simulations for the Ripple

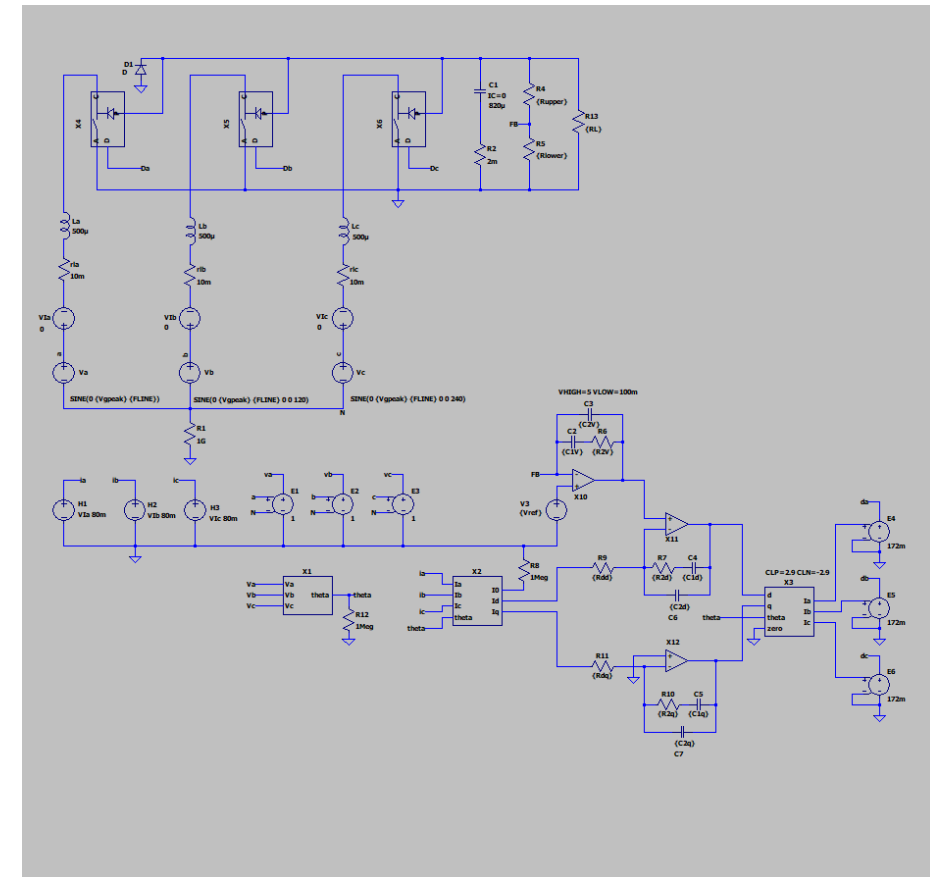
- Part of the output capacitor rms current depends on the low-frequency component
- There is no low-frequency ripple in a balanced, 3-phase, active PFC



Single-phase BCM averaged model



No low-frequency ripple in 3-phase



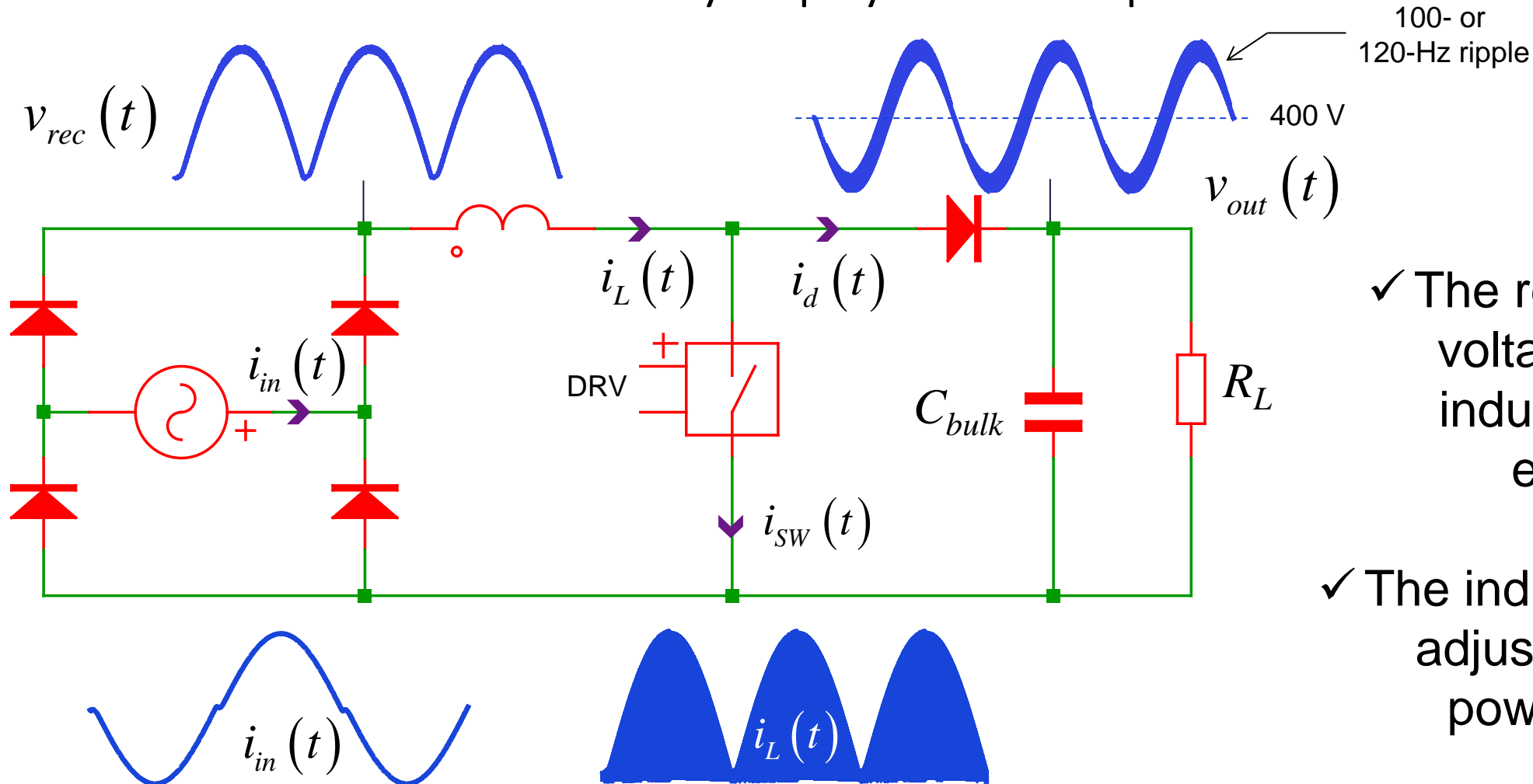
Three-phase BCM averaged model

# Agenda

- Notions of Power Factor
- **PFC Architectures**
- Processing Power – Single Phase
- Processing Power – Three Phases

# Power Factor Correction – One Phase

- An active PFC forces a sinusoidal current absorption in phase with the voltage
- A boost converter is traditionally employed for this operation



- ✓ The rectified input voltage sets the inductor current envelope
- ✓ The inductor current is adjusted to match power demand

# No Diode Bridge with Totem-Pole PFCs

- The bridge hampers overall efficiency with two permanently-conducting diodes



$$P_d \approx 2V_f I_{d,avg}$$

$$I_{F,avg} = \frac{2 \sqrt{2} P_{out}}{\pi V_{ac,LL} \eta}$$

$$P = 300 \text{ W}$$

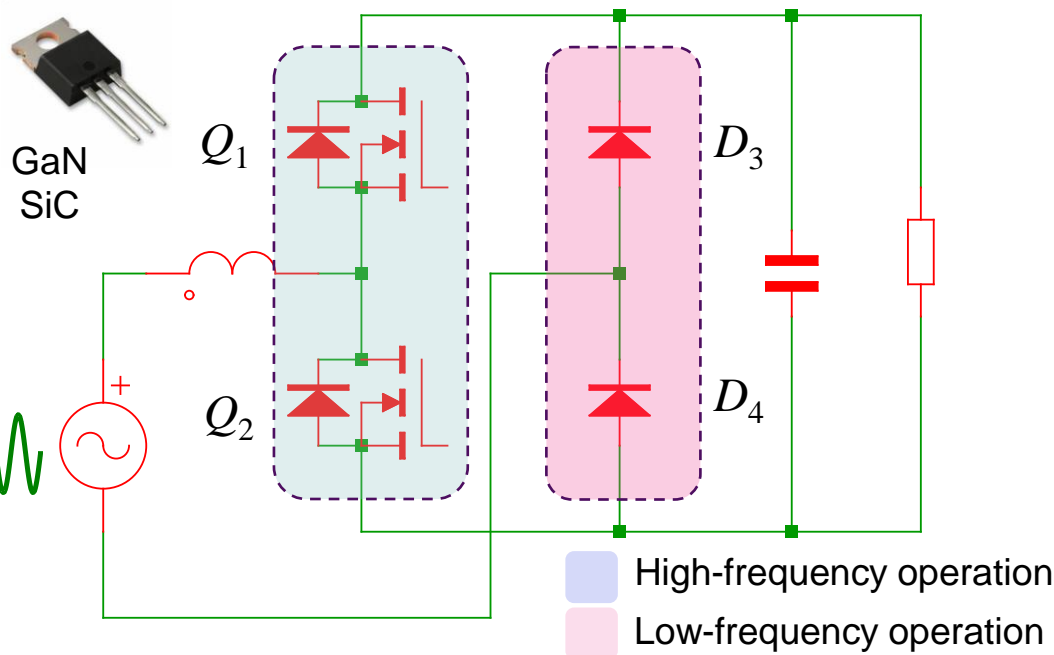
$$\eta = 100\%$$

$$V_{ac,LL} = 90 \text{ V rms}$$

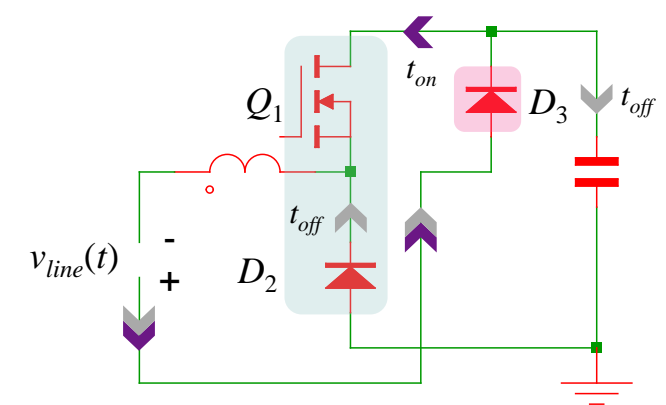
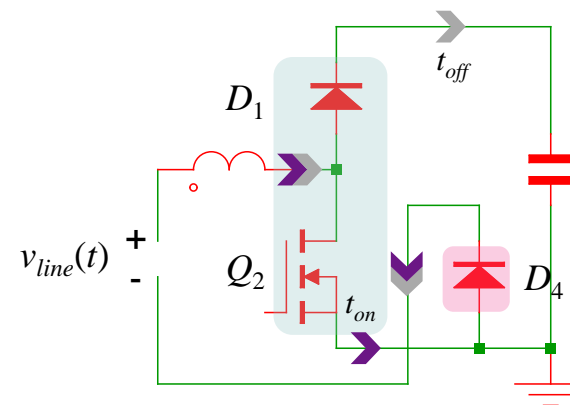
$$P_d \approx 5 \text{ W}$$

$$\text{Eff. loss} \approx 1.7\%$$

- The totem-pole PFC processes the positive and the negative input cycles

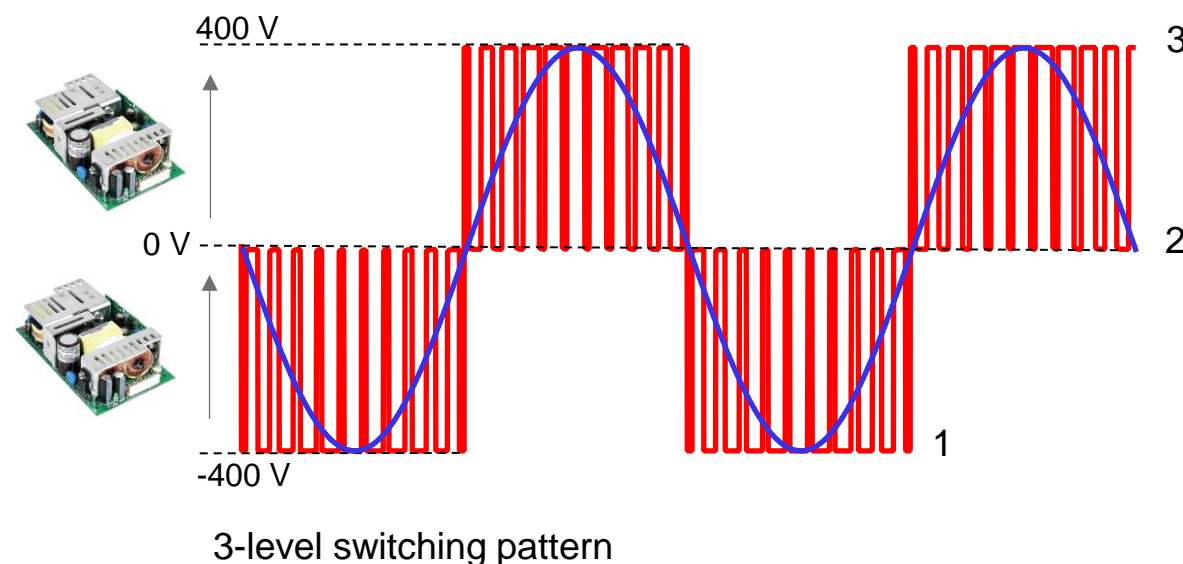
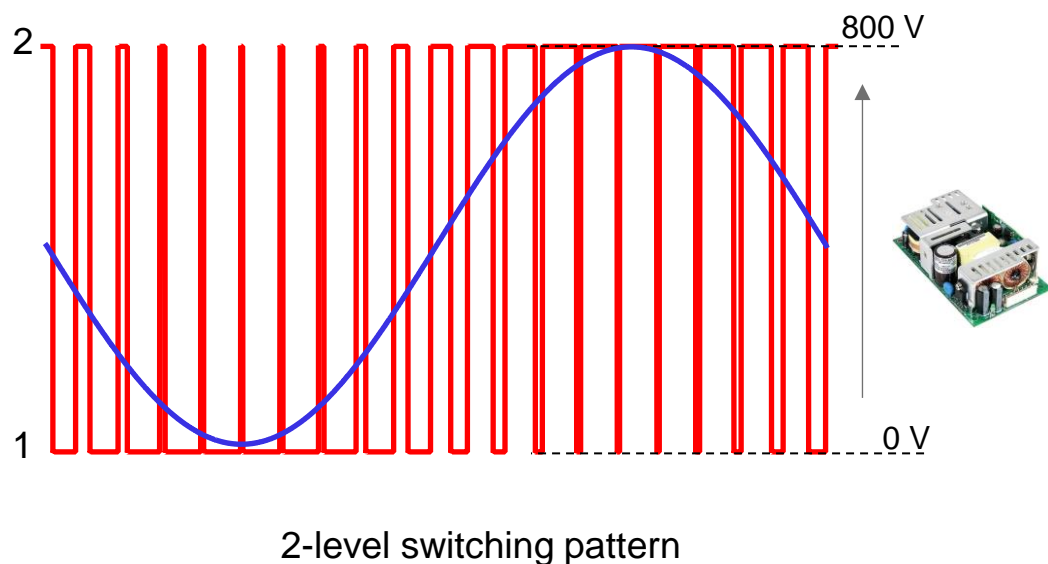


- ✓  $Q_1/Q_2$  swap roles between switches and diodes
- They operate at high frequency: *fast leg*
- ✓  $D_3/D_4$  are active during half of the line cycle
- This is the *slow leg* which can be sync-rectified



# Multi-Level Converters

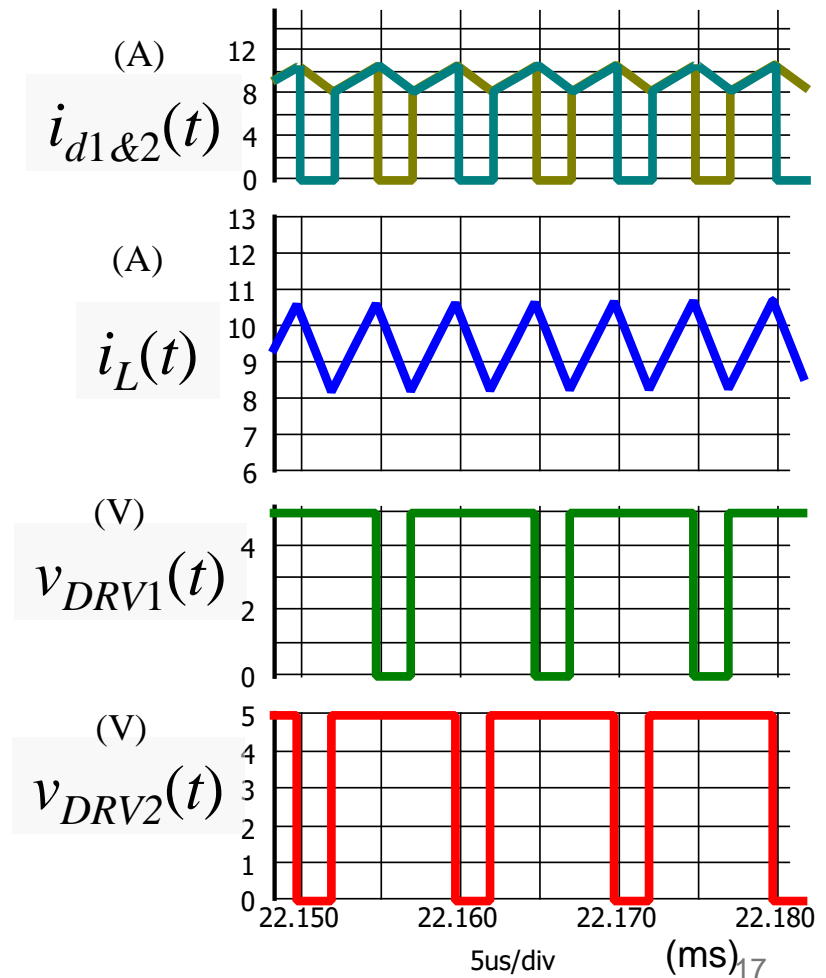
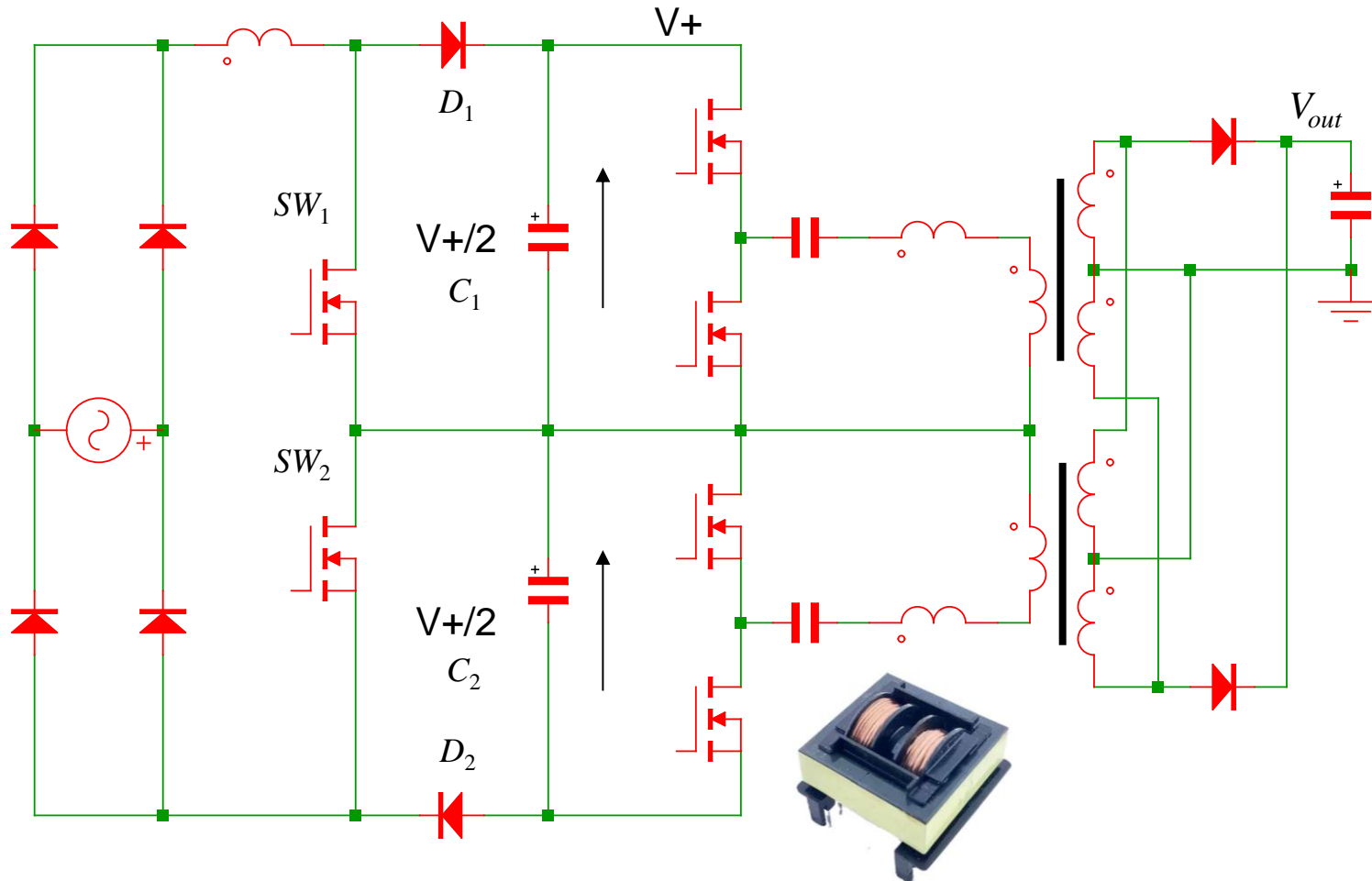
- The classical boost structure delivers a single output voltage of 800 V
- ✓ It is called a *two-level* inverter, meaning the switching pattern is unipolar
- An intermediate 0-V level can be added to form a *three-level* inverter
- ✓ The switching pattern becomes bipolar and transitions via a 0-V state



➔ Stack converters supplied by 400-V rails and reduce semiconductors stress

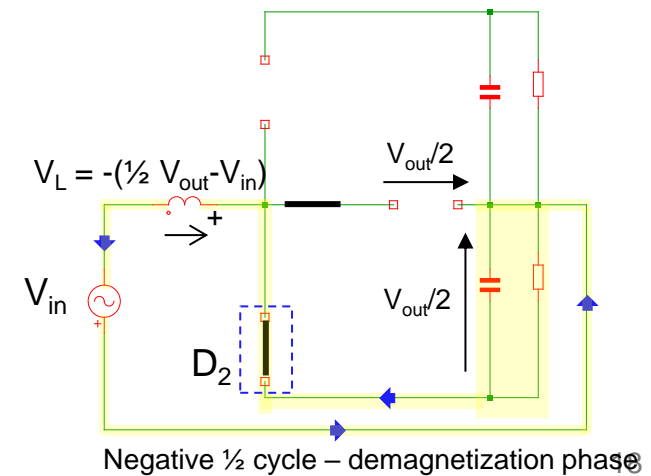
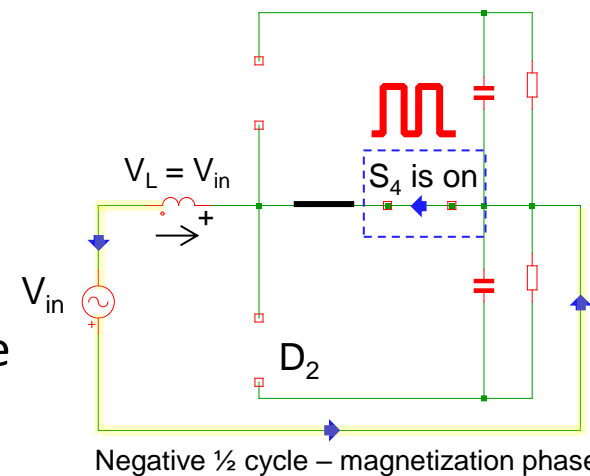
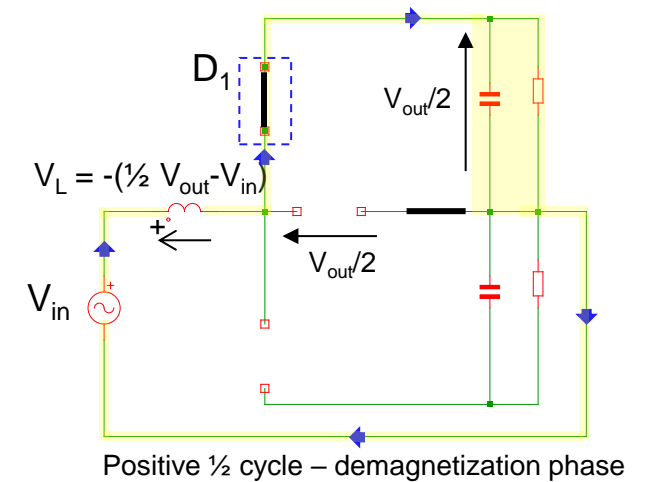
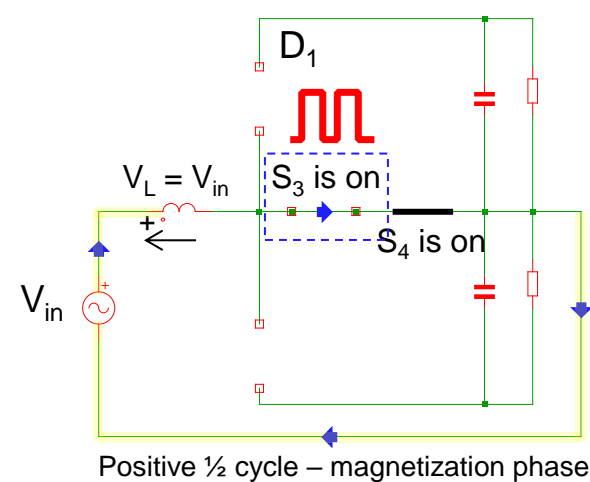
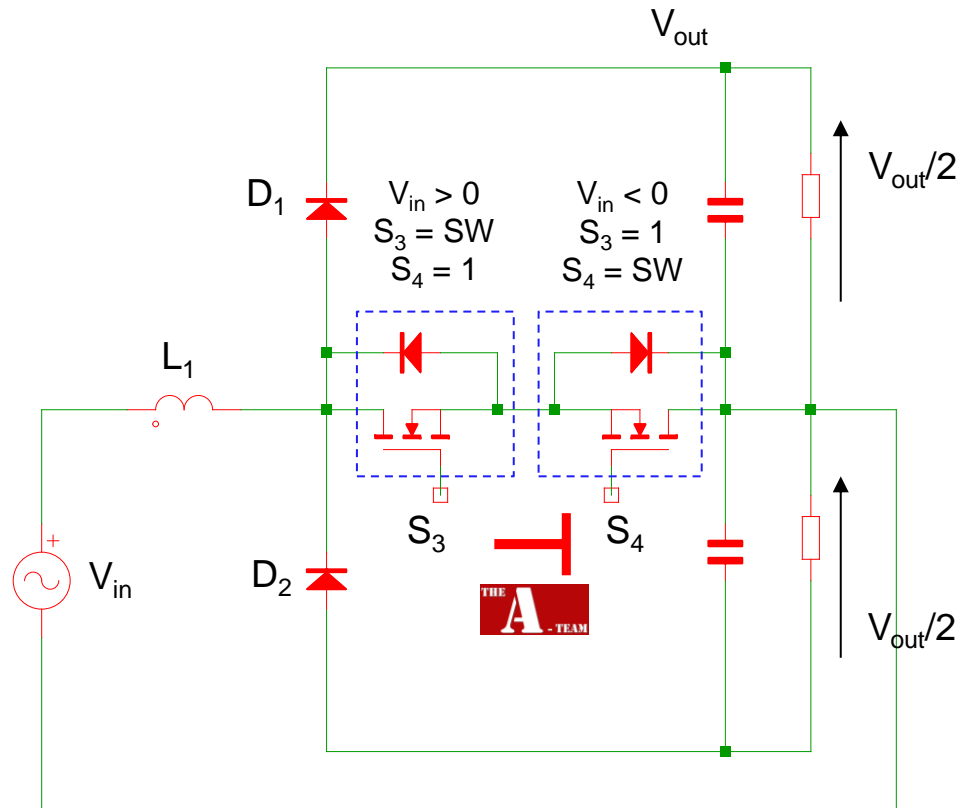
# Stacking High-Power Converters

- The two dc rails of equal values let you use semiconductors of lower voltage
- The output transformers can then be serialized or paralleled for more power



# Three-Level T-Type PFC

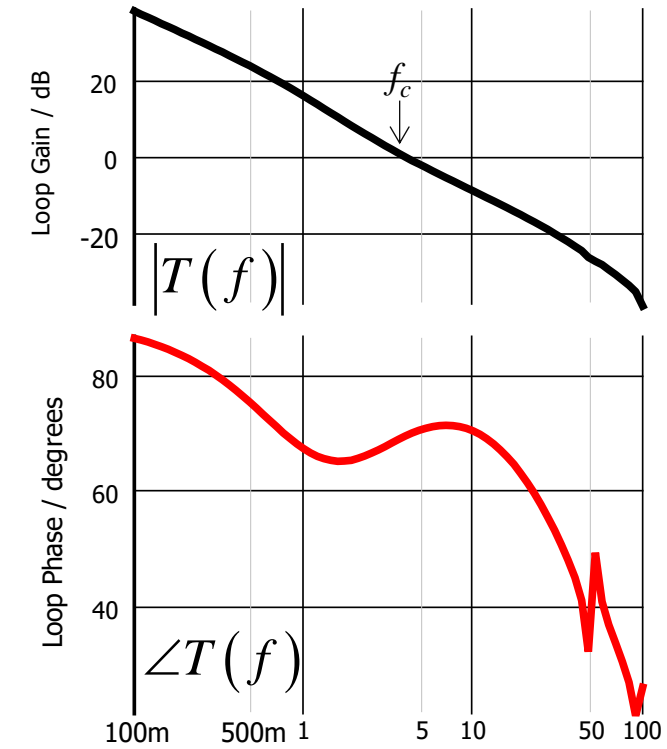
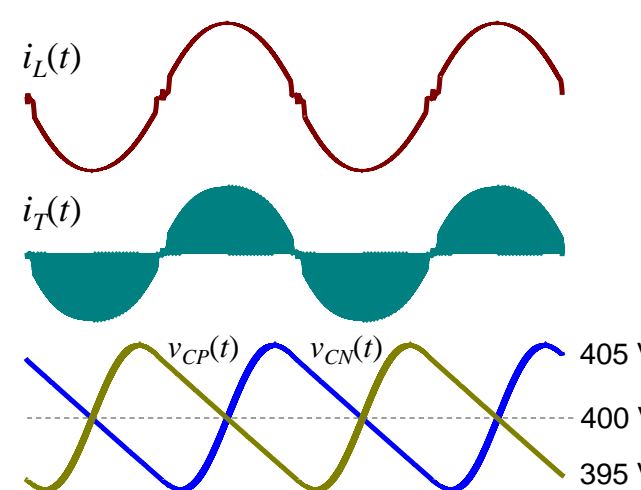
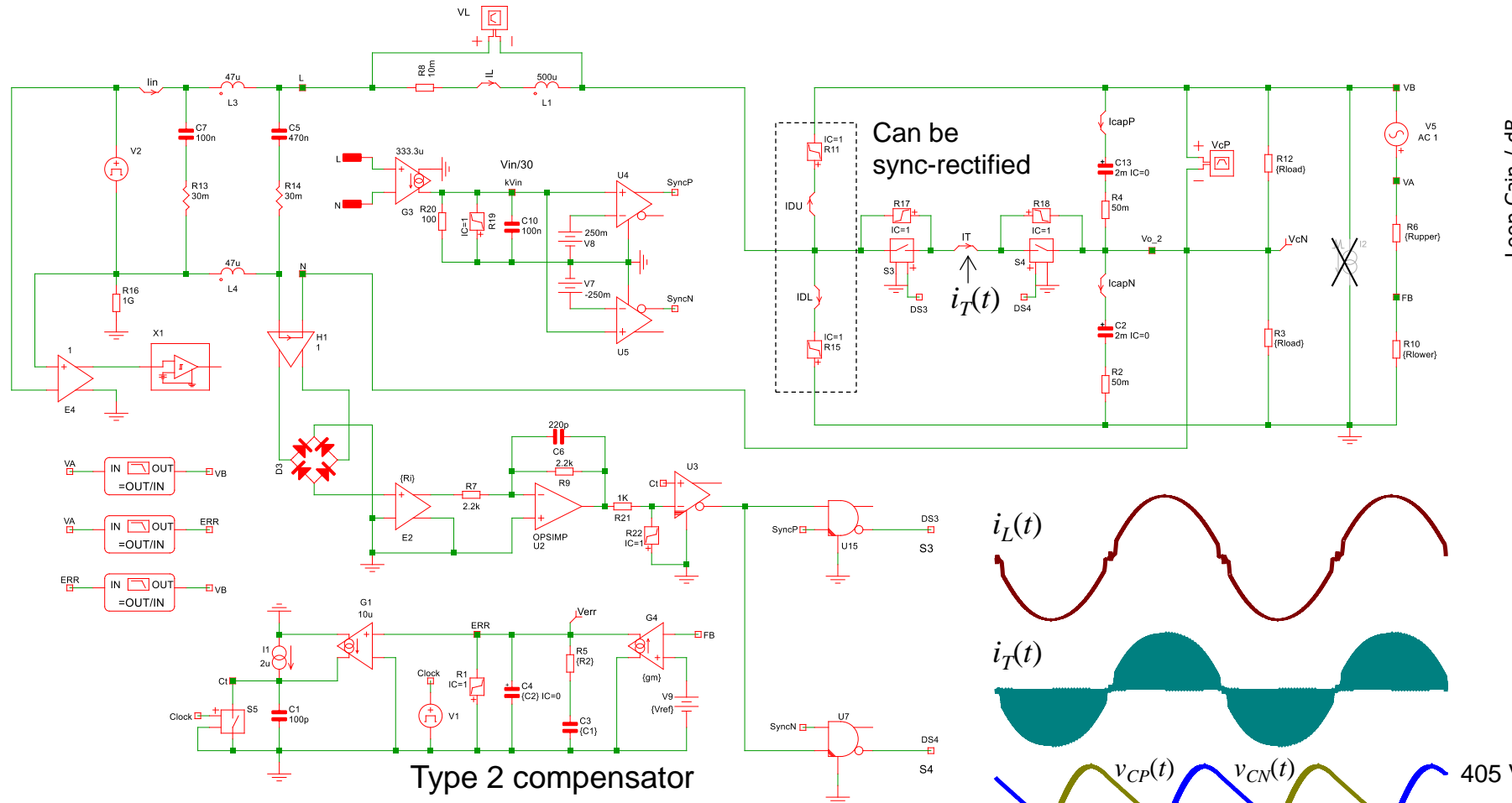
- A 3-level PFC can be implemented by adding a bidirectional switch
- The two T switches operate at high frequency and block  $V_{out}/2$



- The off-time voltage is half of the output voltage
- ✓ Design with a smaller inductor for same ripple

# SIMPLIS Delivers the AC Response

- You can stabilize and test the transient response with the same circuit

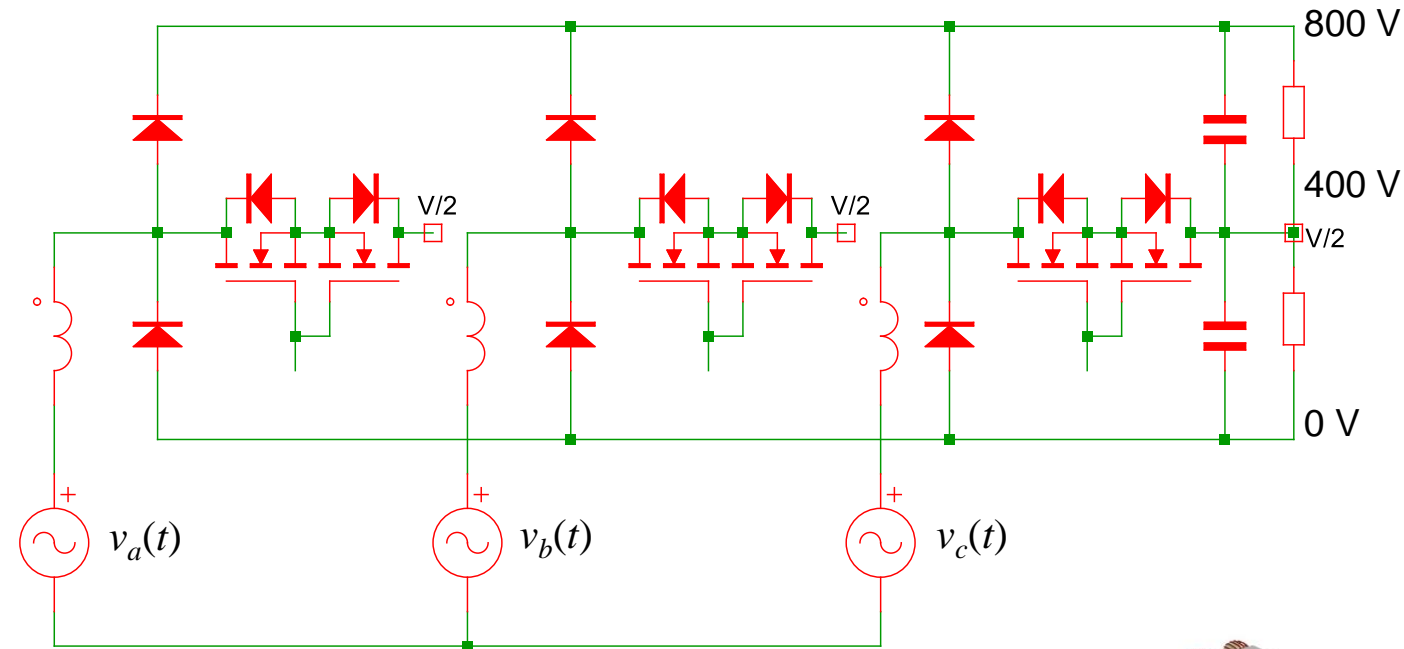
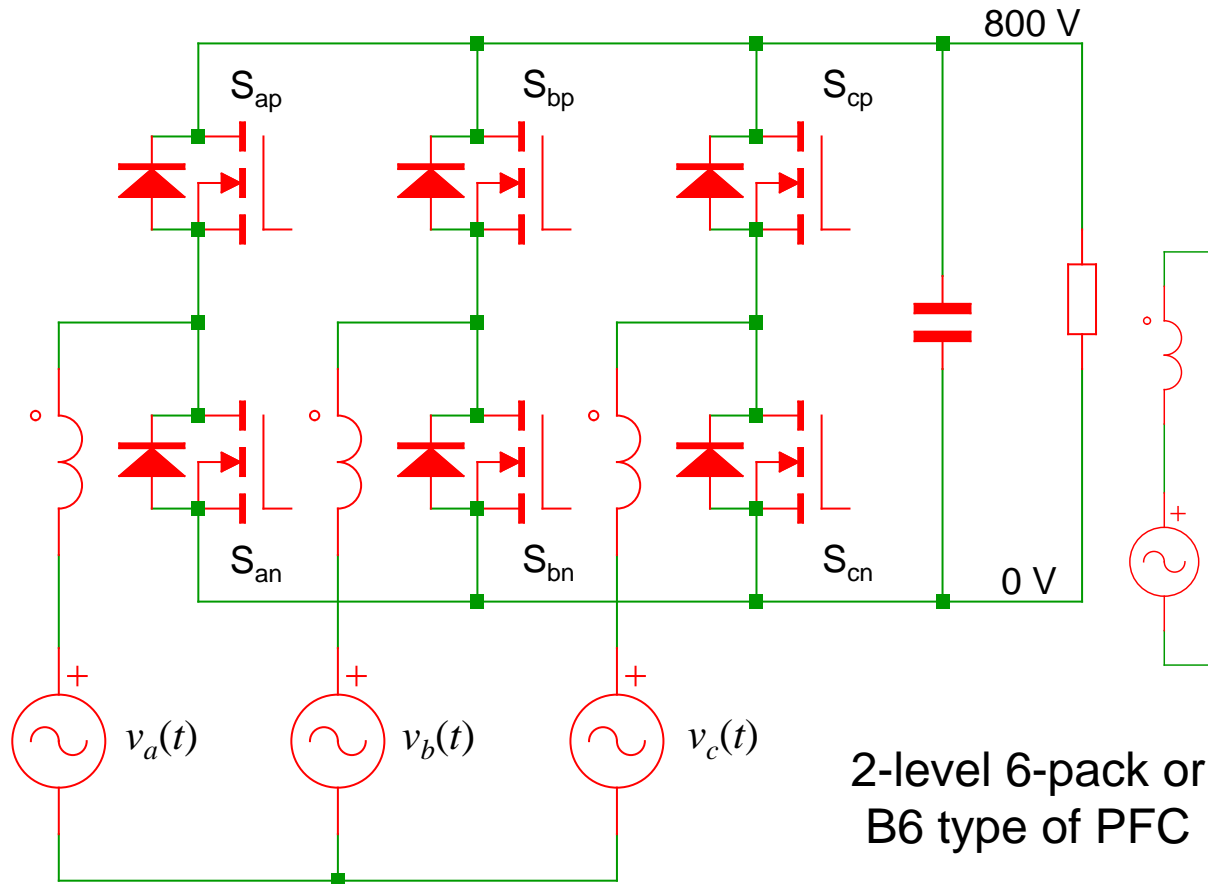


Loop Gain	Gain Crossover Frequency	4.1443925Hz
Loop Gain	Gain Margin	***ERROR***
Loop Phase	Phase Margin	69.969047degrees

$V_{in} = 230 \text{ V rms}$   $P_{out} = 1.5 \text{ kW}$

# Power Factor Correction – Three Phases

- There are three active branches, with or without synchronous rectification
- Different control techniques exist to maximize efficiency and minimize distortion



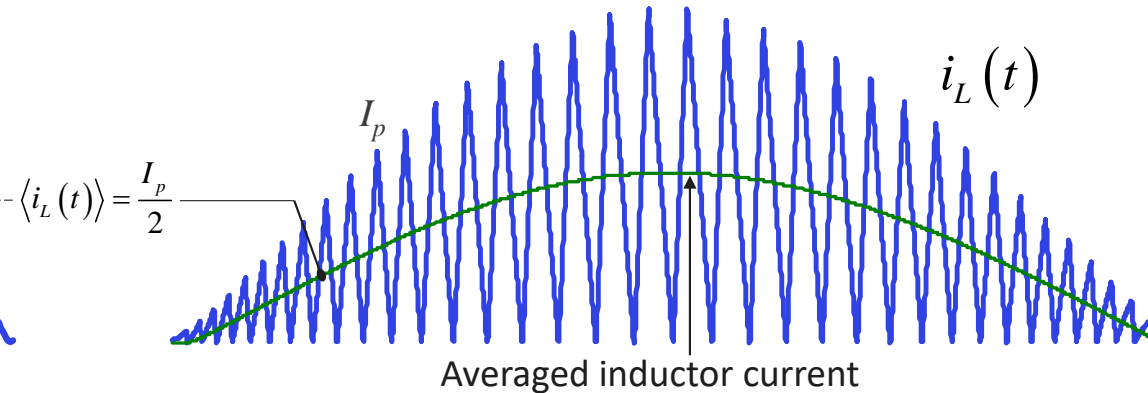
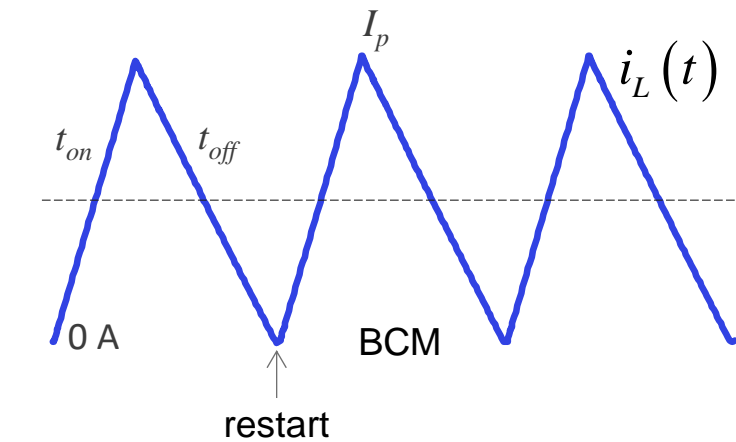
30 kW

# Agenda

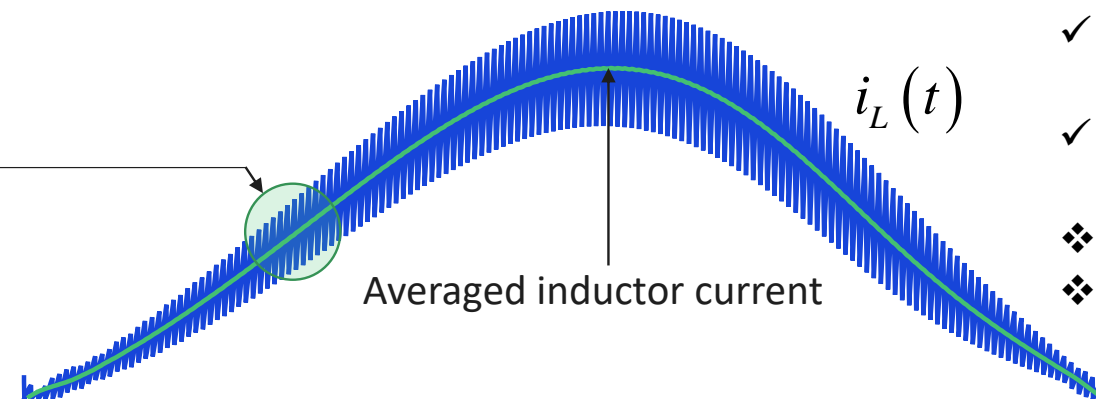
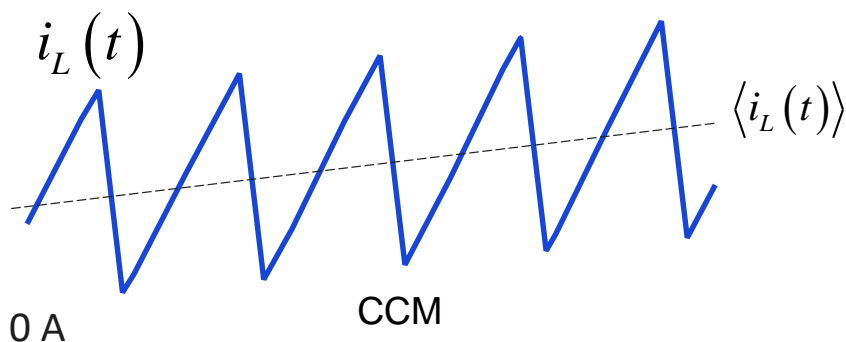
- Notions of Power Factor
- PFC Architectures
- **Processing Power – Single Phase**
- Processing Power – Three Phases

# Borderline or Continuous Operation?

- A PFC can operate in discontinuous, borderline or continuous conduction modes
- Borderline or critical mode suits low to moderate output power levels, below 300 W
- Continuous conduction mode is adopted for high-power converters, above 500 W



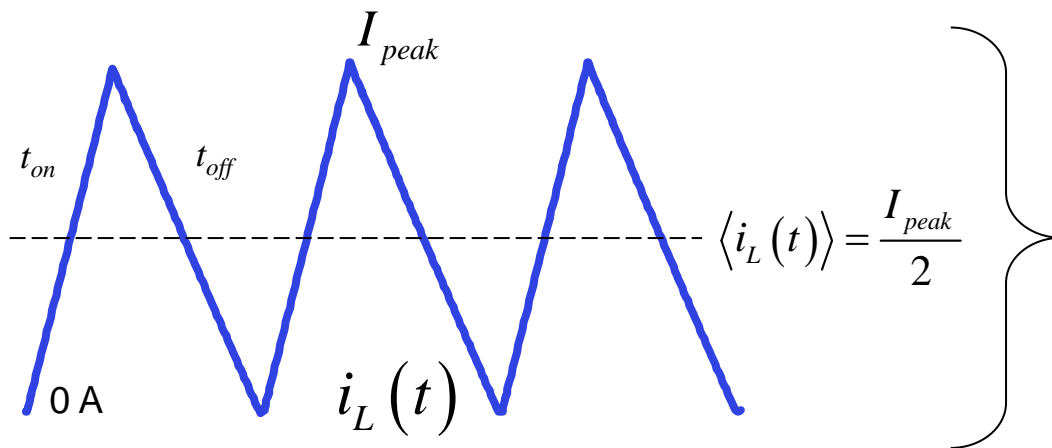
- ✓ Near ZVS switching
- ✓ No  $t_{rr}$  loss on the diode
- ❖ Variable frequency
- ❖ Large rms currents



- ✓ Low ripple reduces core losses and rms currents
- ✓ Average current mode for best distortion figure
- ❖ Large inductance value
- ❖  $t_{rr}$ -related losses due to diode – SiC is popular

# Constant On-Time Control

- Voltage-mode control offers the easiest implementation for BCM PFCs
- ✓ Start with the inductor instantaneous current waveform:



$$p_{in}(t) = v_{in}(t) i_{in}(t) = v_{in}(t) \frac{i_{L,peak}(t)}{2}$$

$$i_{L,peak}(t) = \frac{v_{in}(t)}{L} t_{on}(t) \quad \Rightarrow \quad p_{in}(t) = \frac{v_{in}^2(t)}{2L} t_{on}(t)$$

$$\langle i_{in}(t) \rangle = \frac{v_{in}(t)}{2L} t_{on}(t) \quad \Leftrightarrow \quad \langle i_{in}(t) \rangle = \frac{v_{in}(t)}{R_{in}} = \frac{v_{in}(t)}{\frac{V_{ac}^2}{P_{in}}}$$

Resistive input

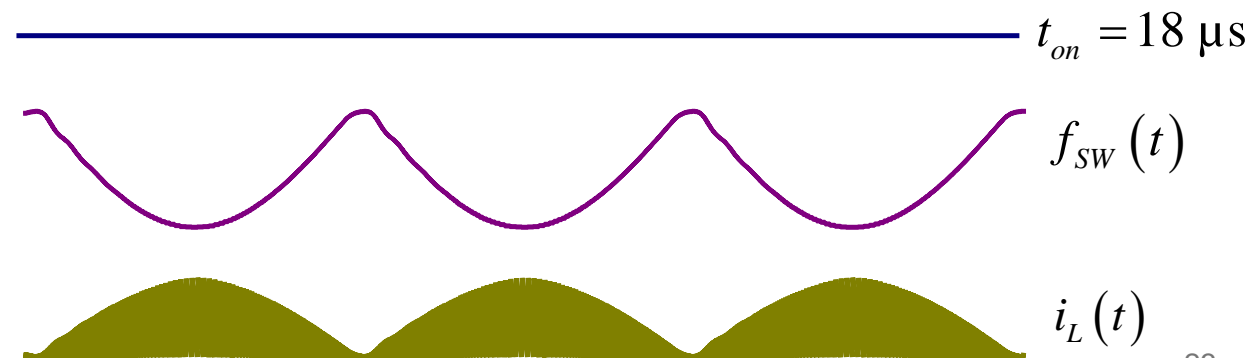
- The power sets the on-time value in relationship with the rms input voltage

$$t_{on} = \frac{2LP_{in}}{V_{ac}^2}$$

$\Rightarrow$ 

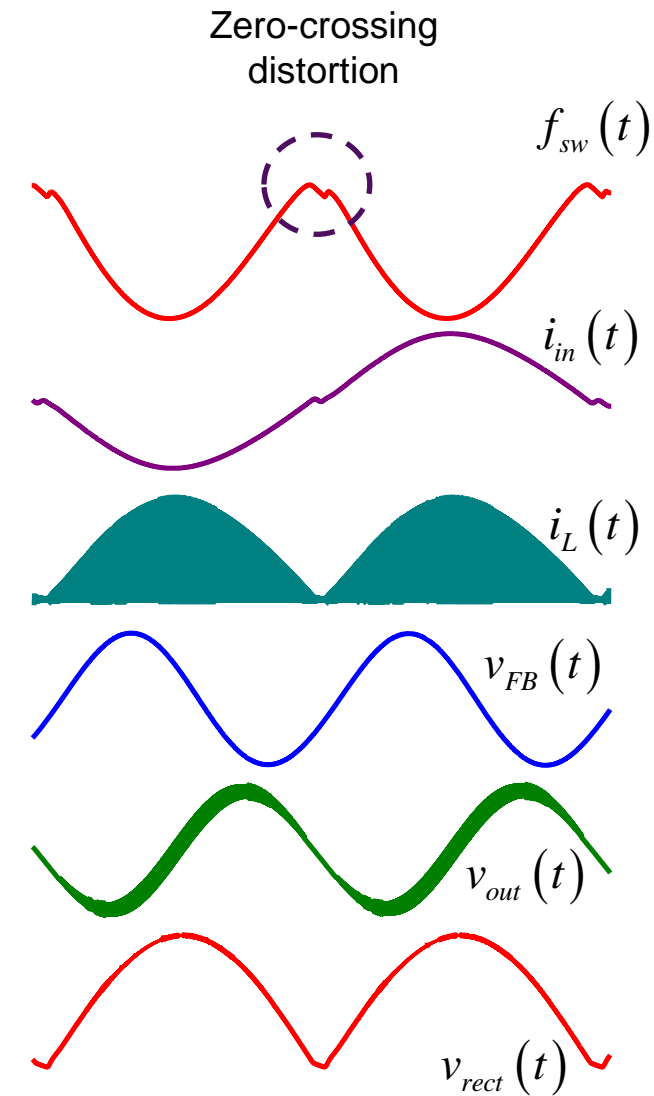
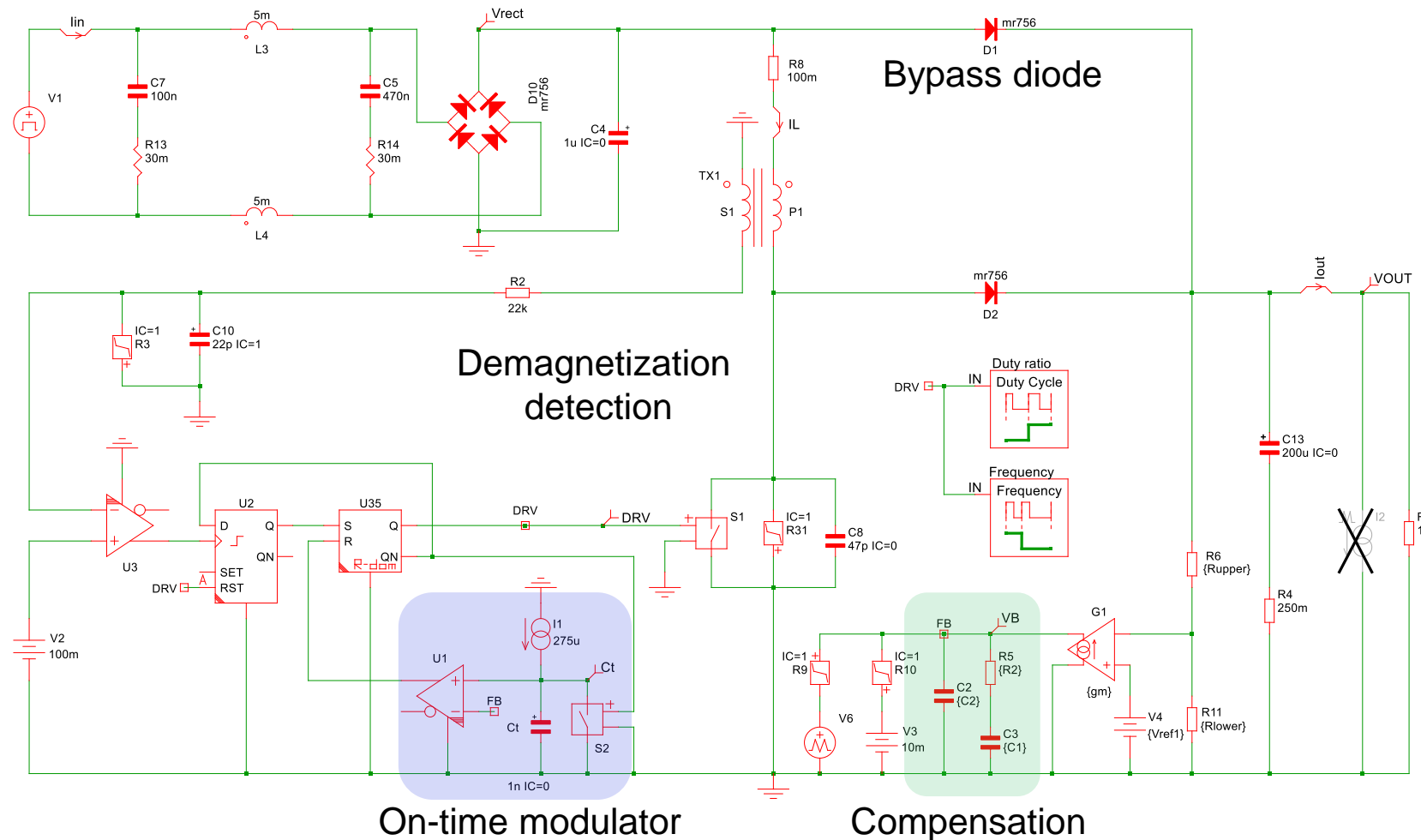
$$i_{in}(t) = \frac{V_{ac} \sqrt{2t_{on}}}{2L} \sin(\omega t)$$
 constant

- ✓ On-time is constant
- ✓ Frequency is variable



# Voltage-Mode Operation

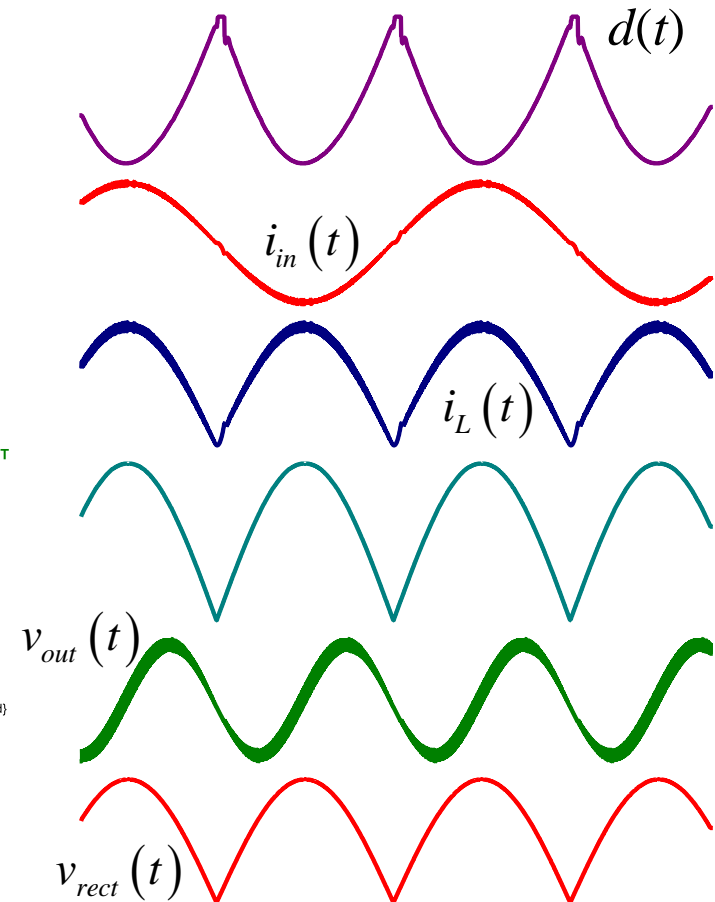
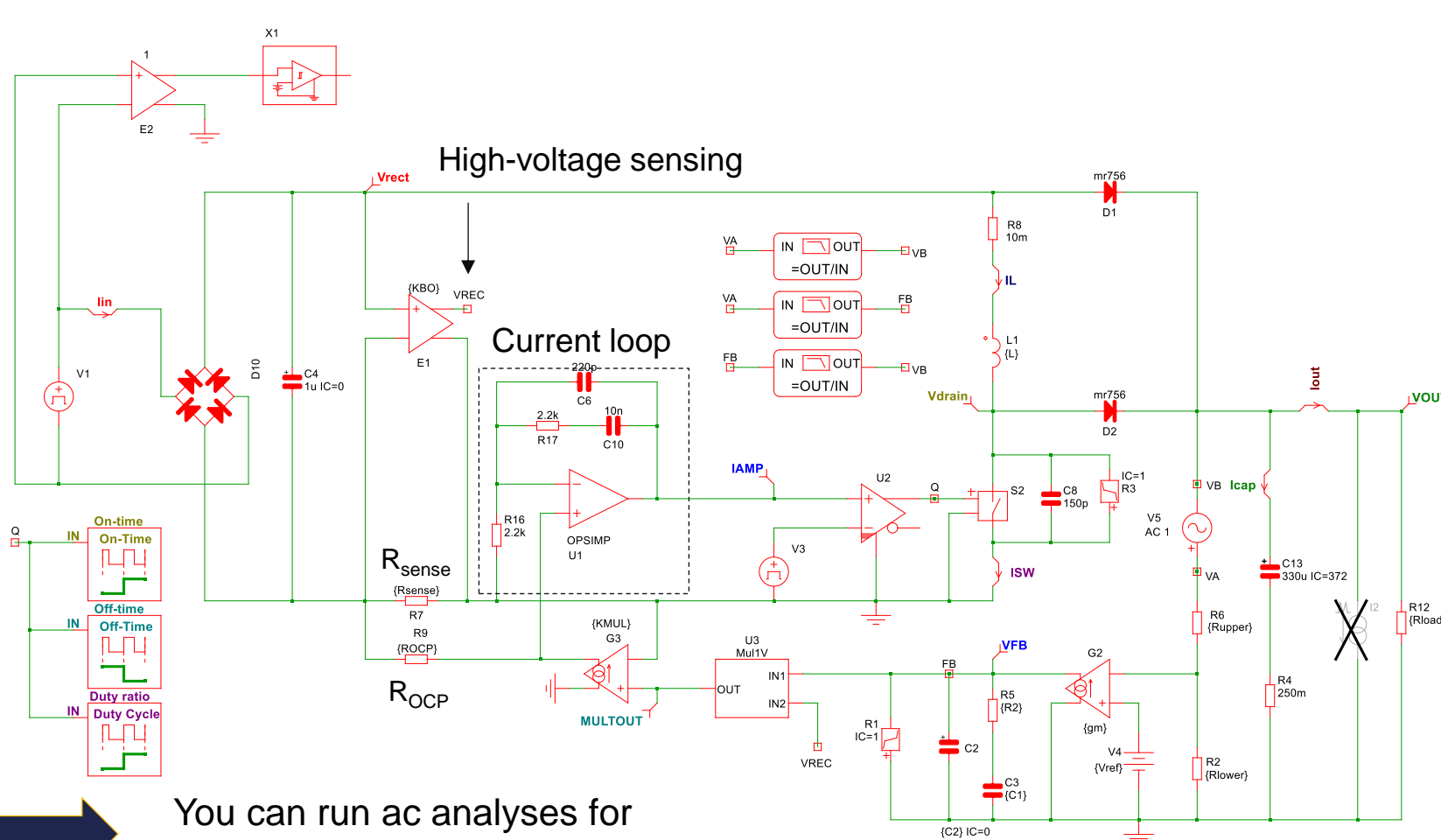
- Constant on-time can be implemented in voltage-mode control
- ✓ No need to sense the input voltage!





# Average Current Mode Control – CCM

- A high-bandwidth loop monitors the inductor current to force sinusoidal waveshape
- A multiplier scales the current envelope to meet output power requirements



You can run ac analyses for current and voltage loops

# Predictive Control Law – No Line Sensing

- It is possible to control the duty ratio without sensing the input voltage
- This elegant approach simplifies the implementation of the PFC engine

In a PFC

$$\langle i_L(t) \rangle = i_{in}(t) \propto v_{in}(t)$$

Dc transfer characteristic:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} = \frac{1}{D_{off}} \rightarrow R_{in} = \frac{V_{in}}{I_{in}} = \frac{D_{off} V_{out}}{\langle i_L(t) \rangle}$$

If  $D_{off}$  is shaped as:

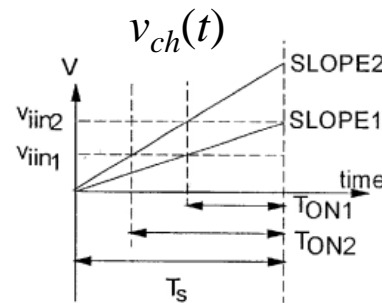
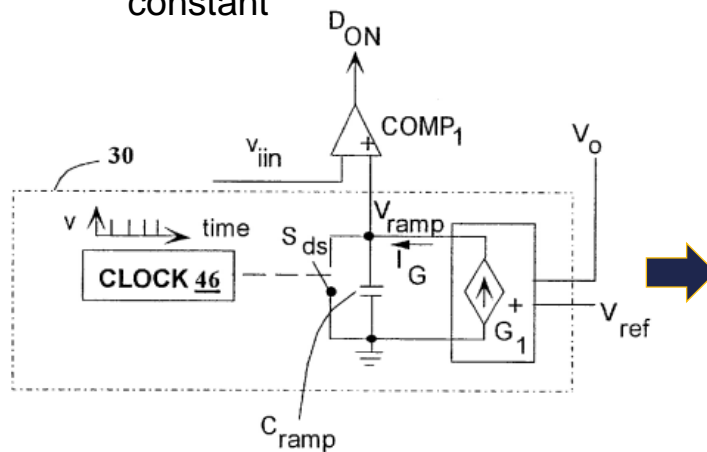
$$D_{off} = \frac{R_{in}}{V_{out}} \langle i_L(t) \rangle$$

It ensures a sinusoidal absorption

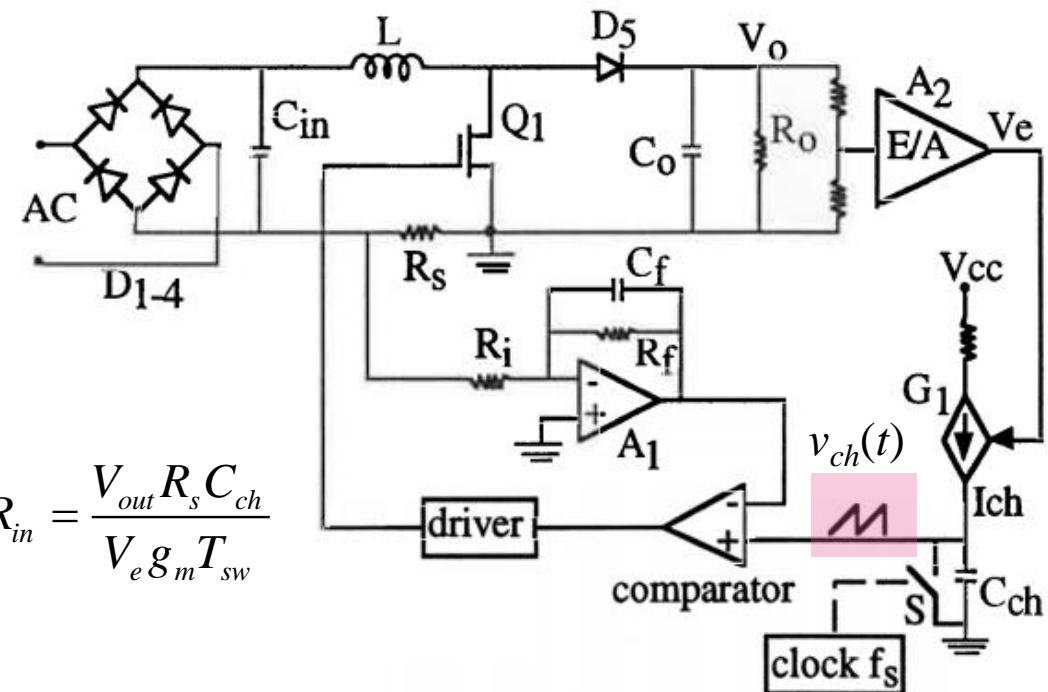
That is, a resistive input will be observed if  $D_{off}$  is programmed according to the rule:

$$D_{off} = \left( \frac{R_e}{V_o(av)} \right) I_{L(av)} \quad , \quad 0 < D_{off} < 1 \quad (4)$$

constant

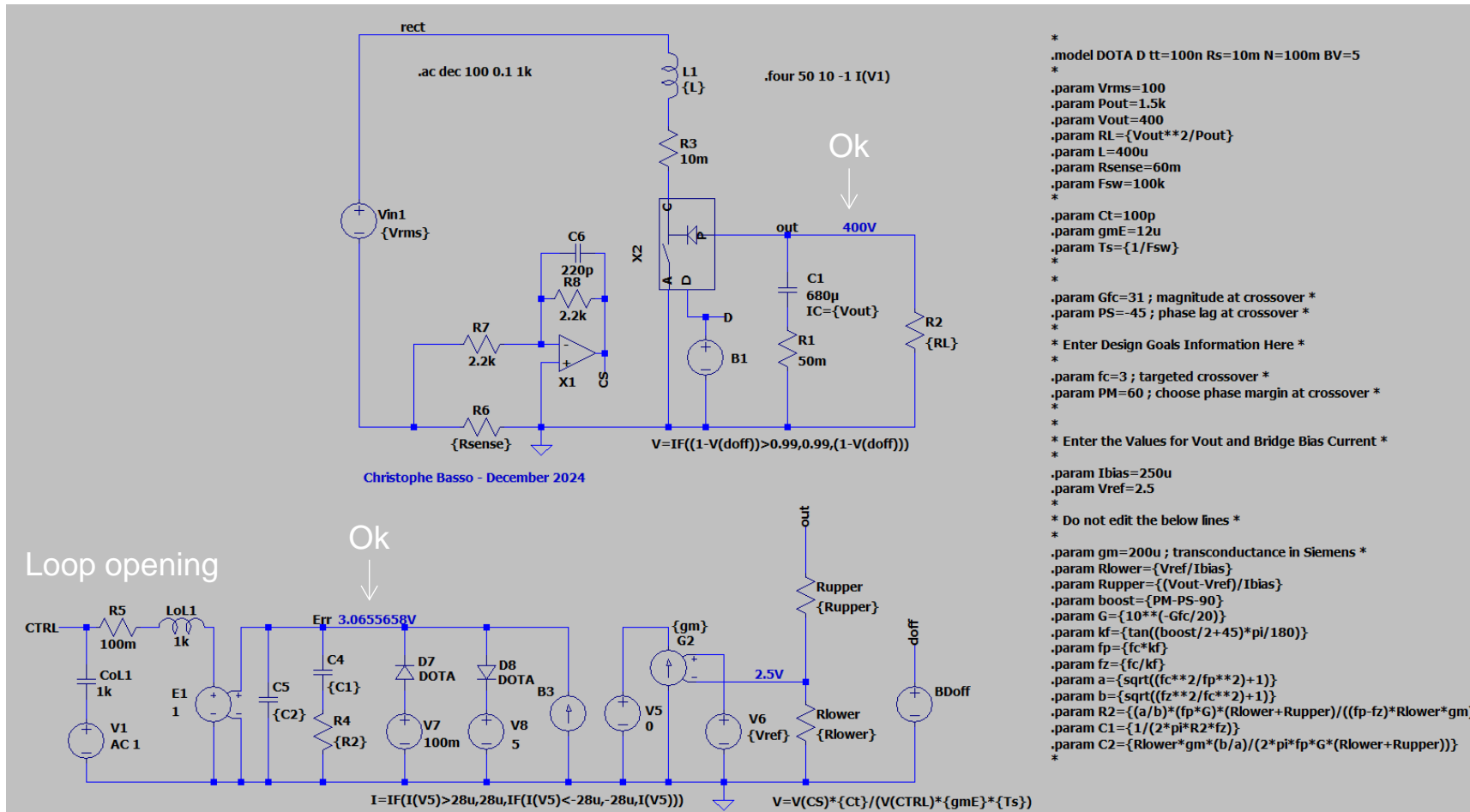


$$R_{in} = \frac{V_{out} R_s C_{ch}}{V_e g_m T_{sw}}$$



# An Averaged Model to Stabilize the Loop

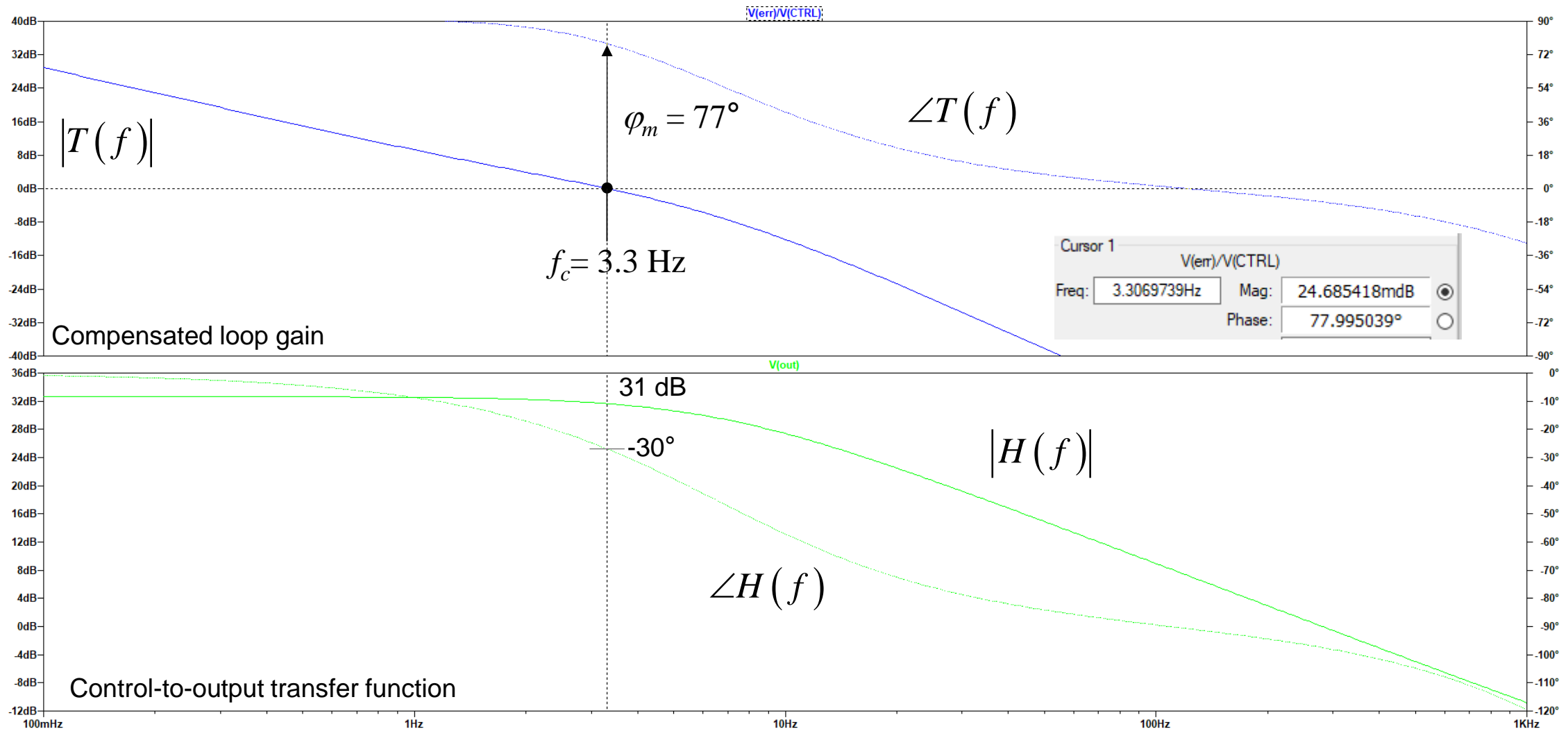
- An average model can be built and offers many advantages for the PFC study
- ✓ It simulates fast (no switching component) and it works for ac analyses



- The right-side macro automates the compensation components values for the type 2 OTA
- Always check the operating points are correct before considering the ac plots
- This is the voltage-loop ac analysis, but the current loop can also be swept

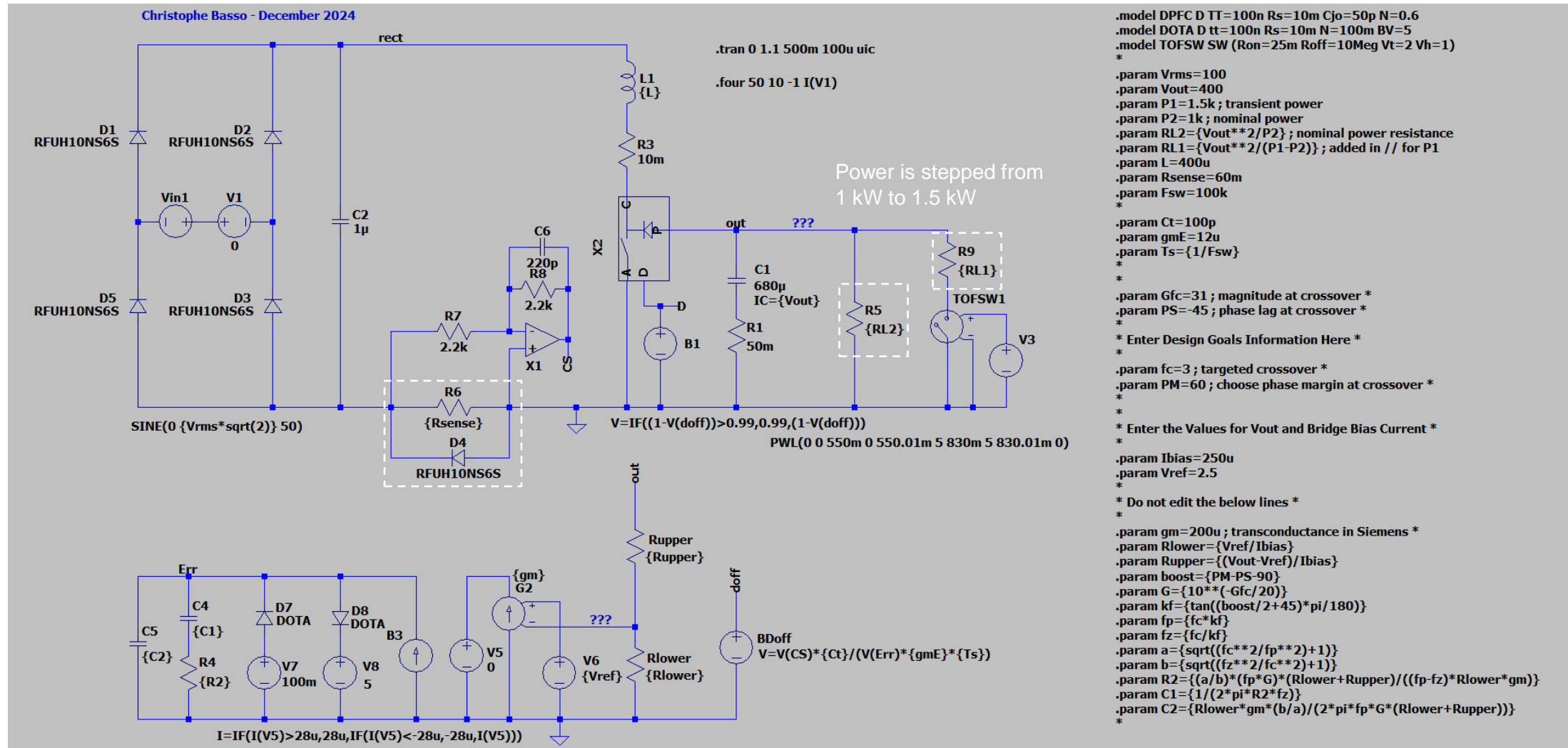
# Check Crossover and Margins are Ok

- SPICE linearizes the large-signal PWM switch model and delivers ac results in a second



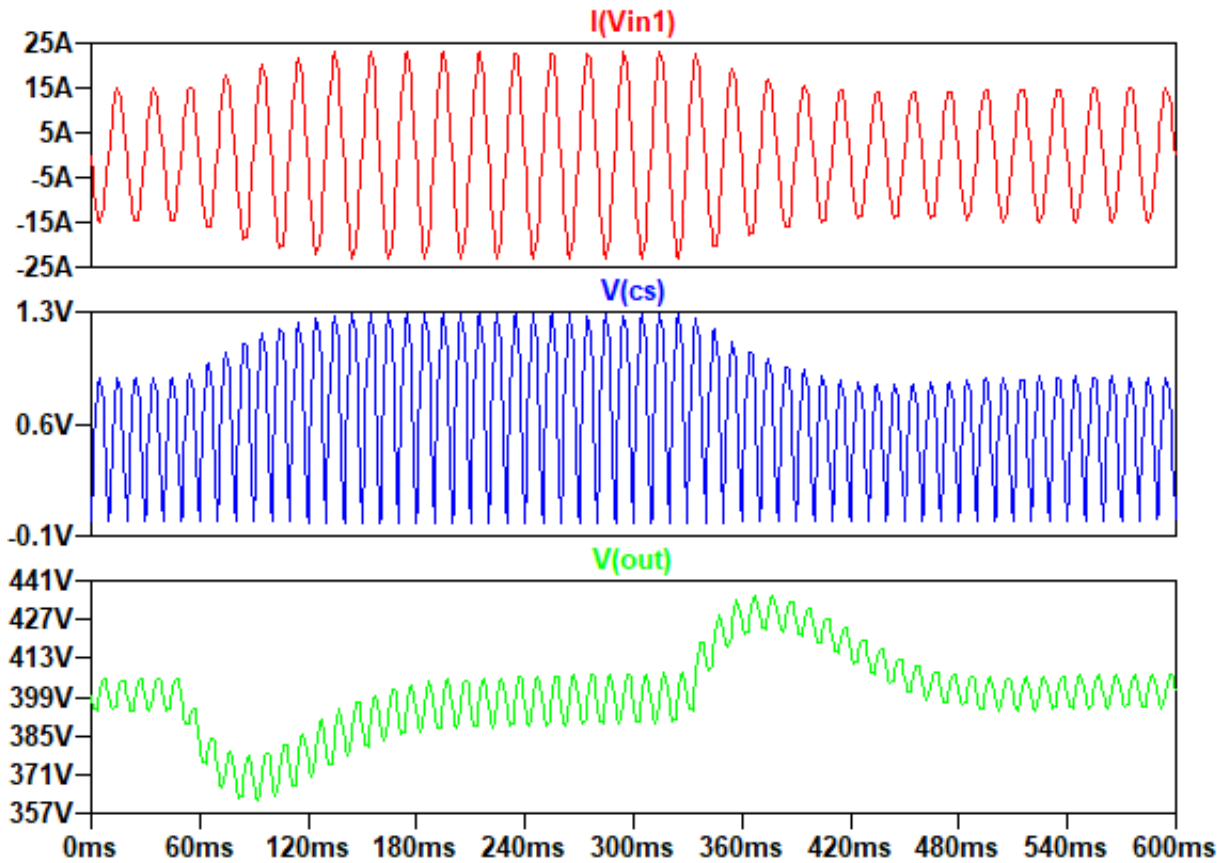
# Averaged Model and Transient Analyses

- Transient analyses are extremely fast and let you test the compensation strategy

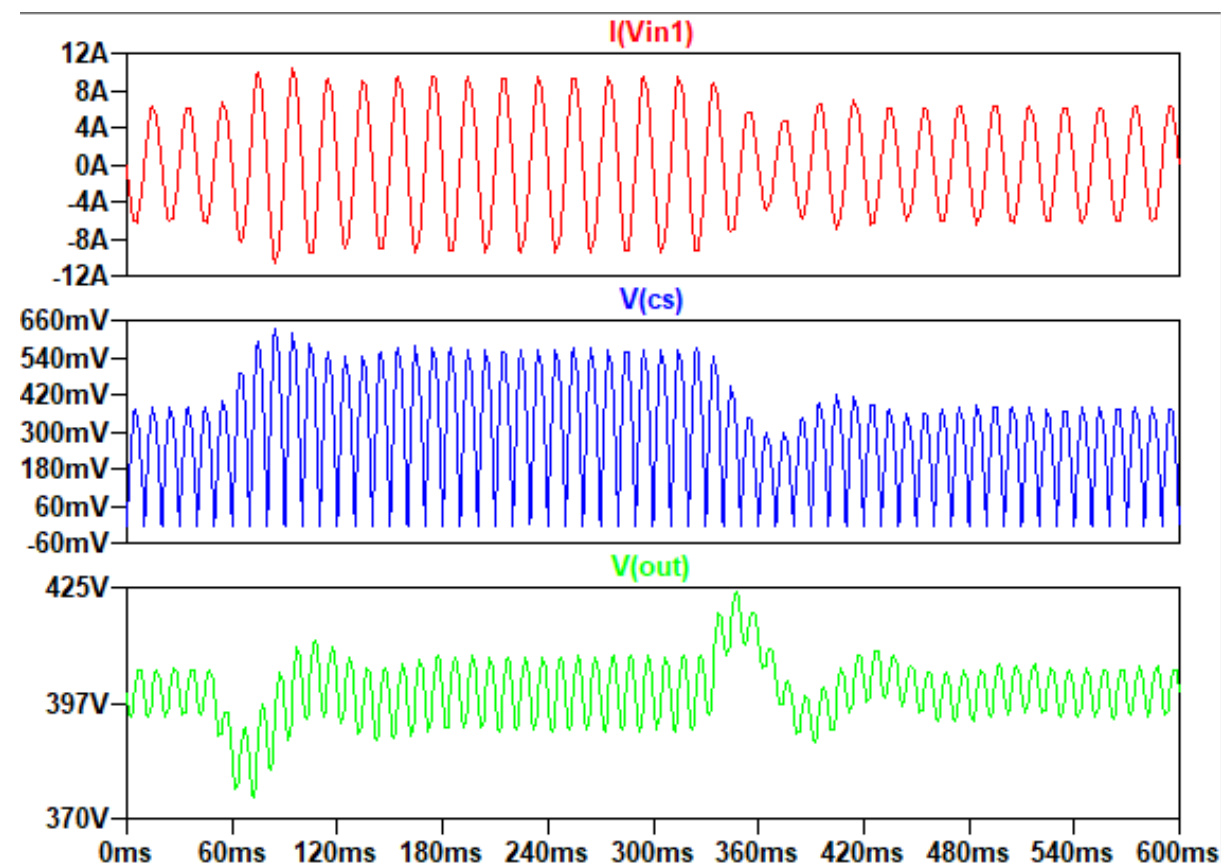


# Testing the Step Load Response

- The output voltage is stable at low line but shows a bit of ringing at high line
- The transient response is better in high line as the crossover frequency increases



$P_{out}$  stepped from 1 kW to 1.5 kW,  $V_{in} = 100 \text{ V rms}$

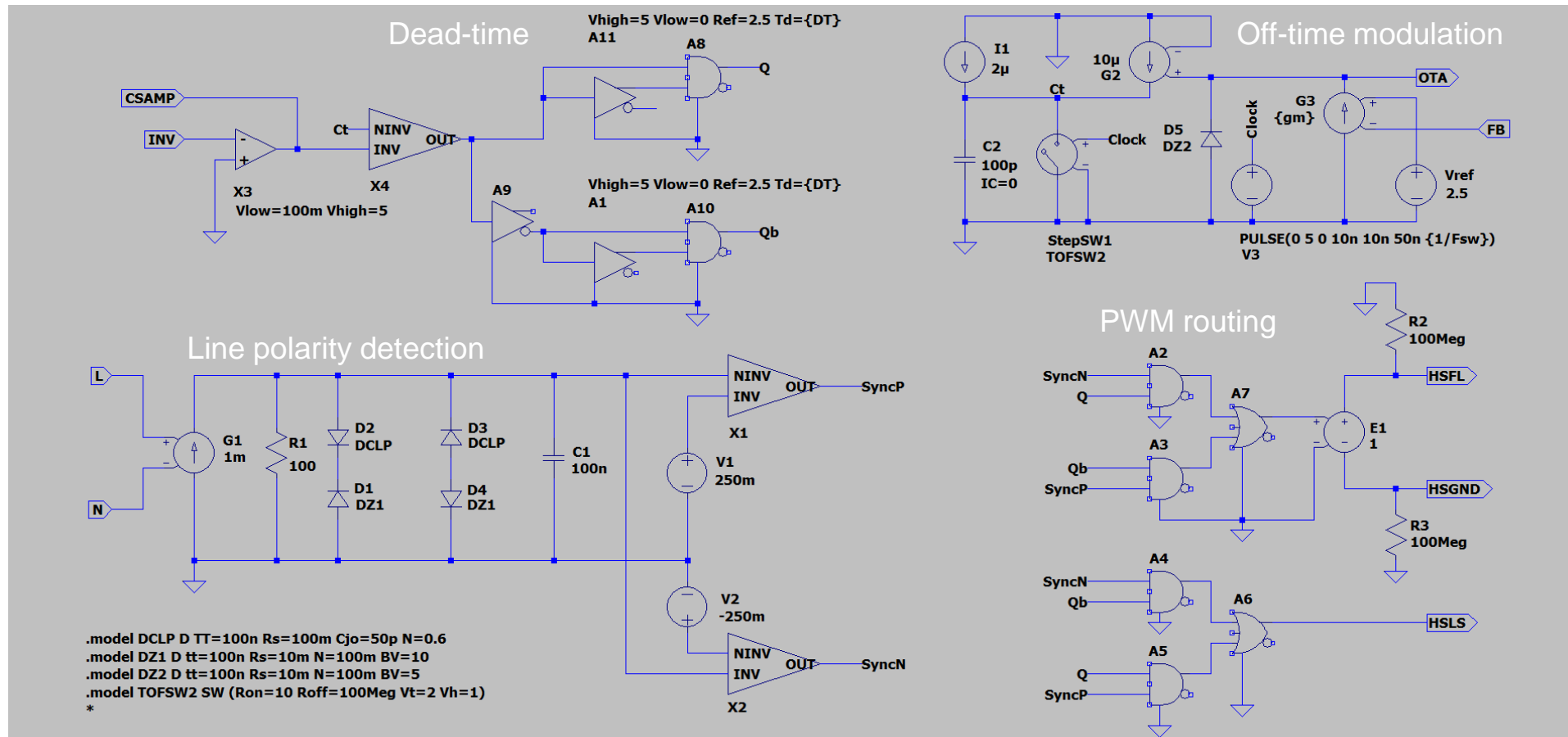


$P_{out}$  stepped from 1 kW to 1.5 kW,  $V_{in} = 230 \text{ V rms}$



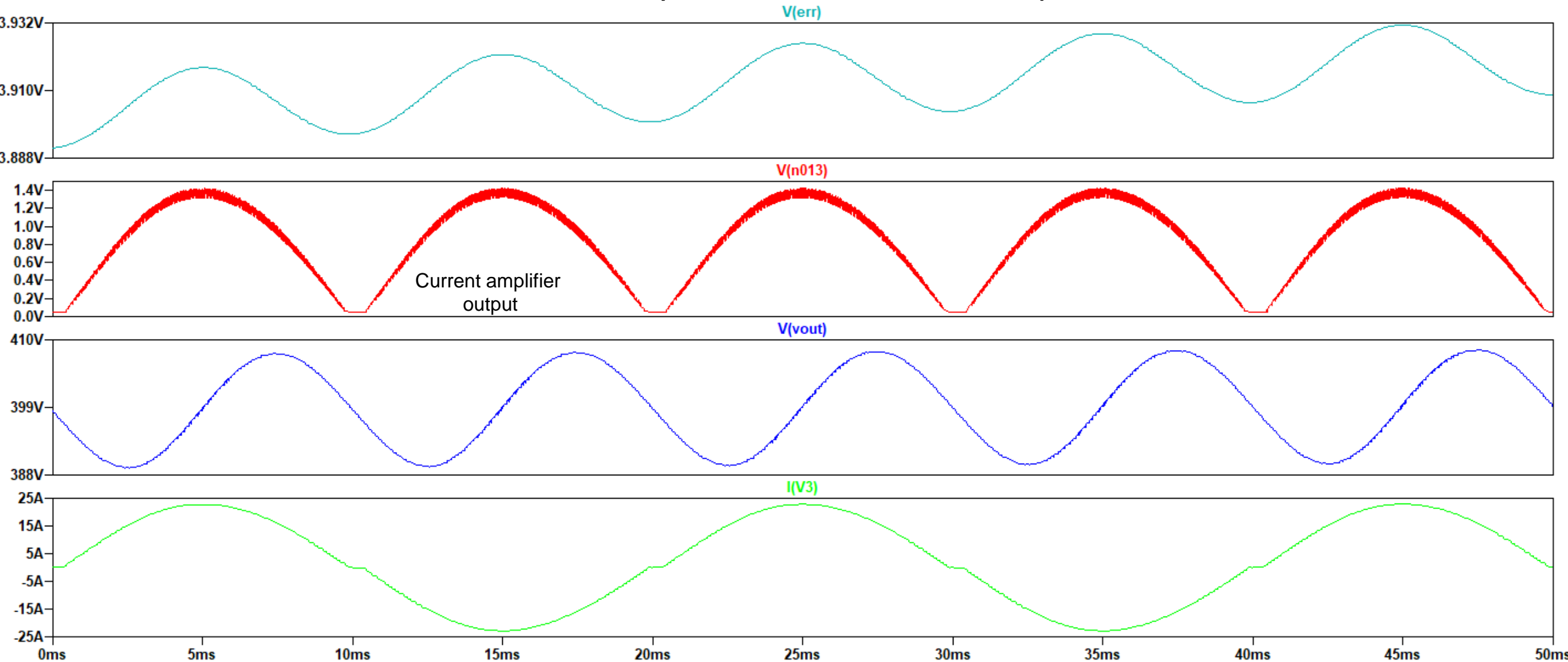
# Inside the TPPFC Subcircuit

- You need to determine the input line polarity to route the PWM signals
- Dead-time is inserted to provide smooth handover between switch and sync rectifier



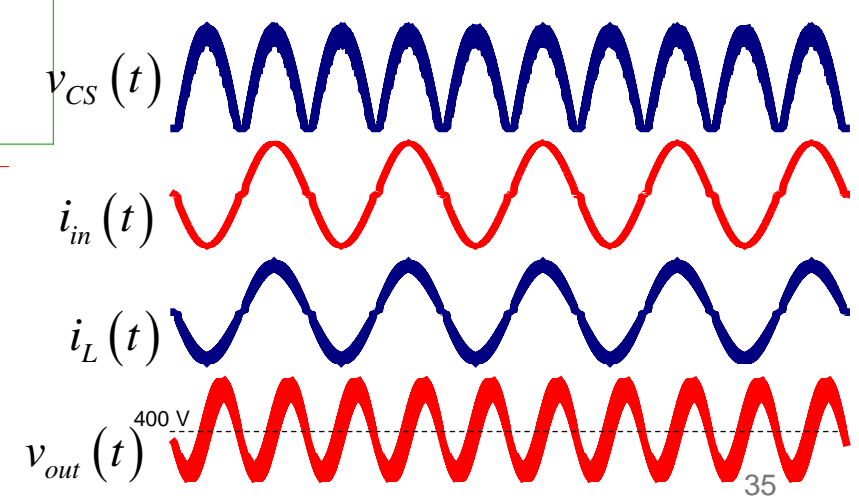
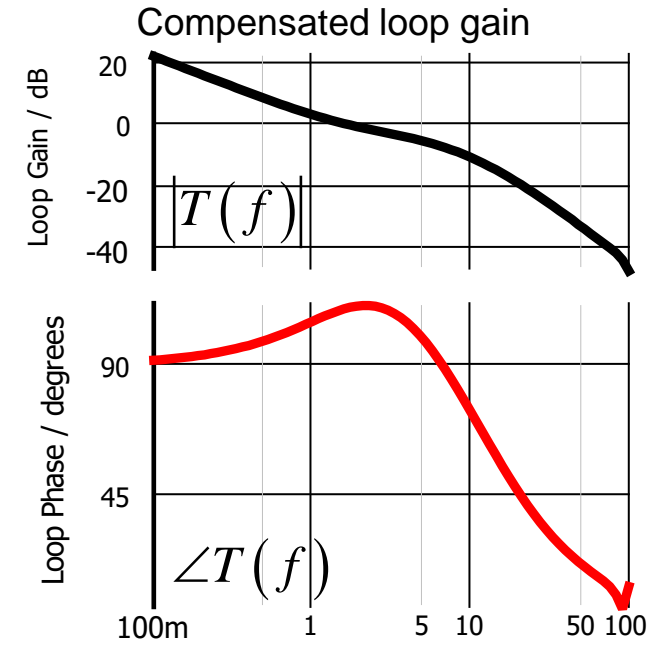
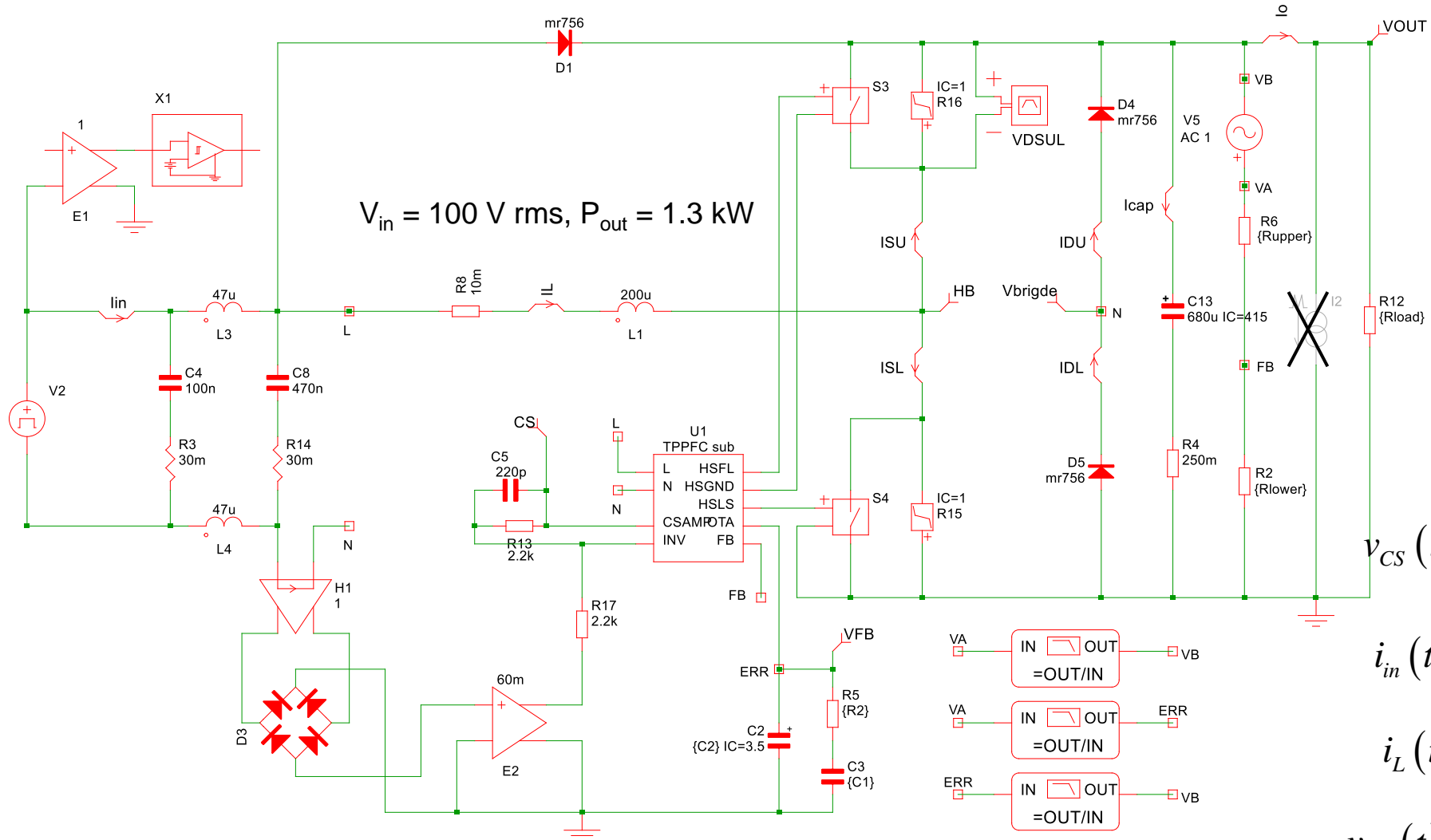
# Operating Waveforms

- The simulation time is 183 s on my machine which is acceptable



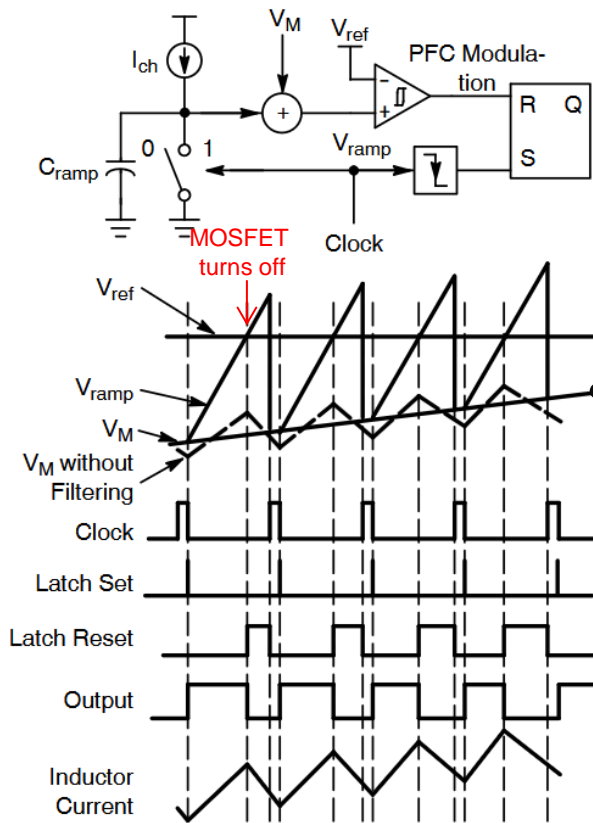
# SIMPLIS for AC and TRAN Responses

- There is no need to resort to an averaged model with SIMPLIS



# NCP1654 – a Different Approach

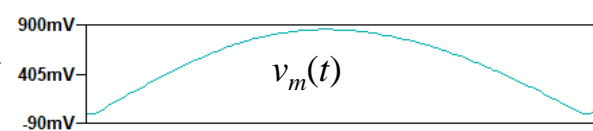
- The NCP1654 from *onsemi* uses a slightly different technique to produce  $1-d(t)$
- The static input voltage is used to scale the control voltage envelope



This is the internal modulator of the NCP1653/54

Boost dc transfer characteristic  $\frac{V_{out}}{V_{in}} = \frac{1}{1-d} \Rightarrow V_{in} = V_{out} (1-d)$

$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{\langle i_L(t) \rangle} = \frac{V_{out}}{\langle i_L(t) \rangle} (1-d)$   $R_{in}$  has to be constant if we want to emulate a resistance



The transition occurs when  $V_{ramp} = V_{ref}$  or:  $V_m + \frac{I_{ch} dT_{sw}}{C_{ramp}} = V_{ref}$

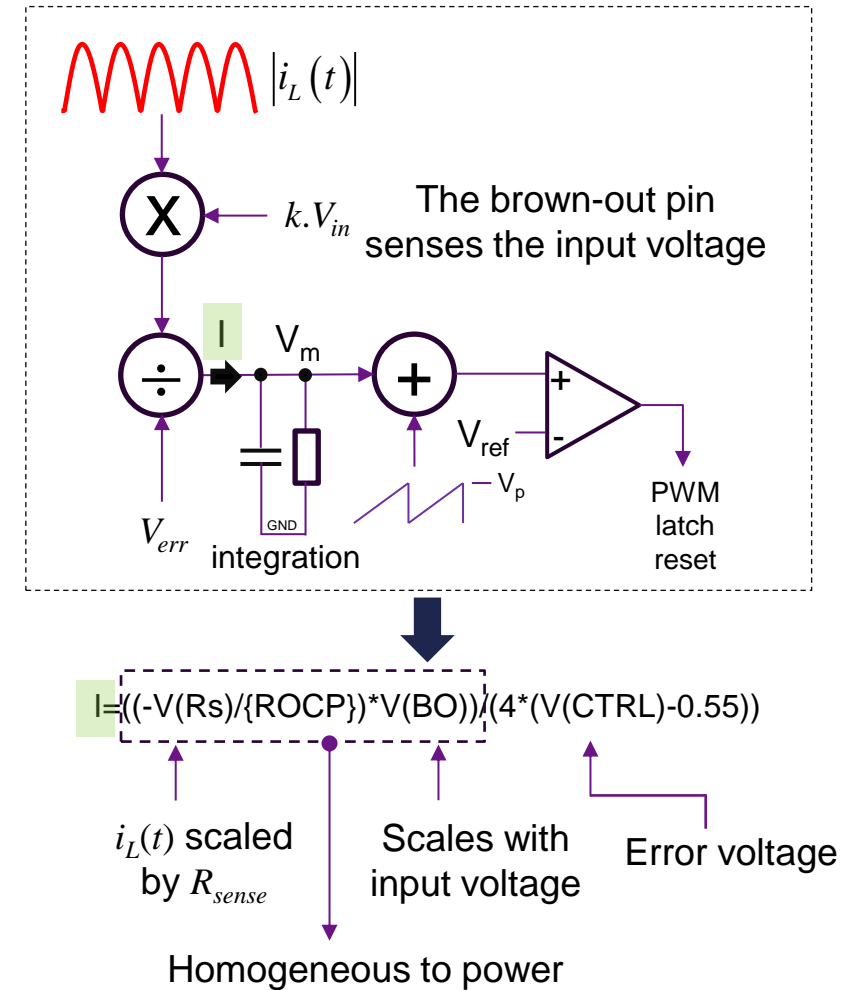
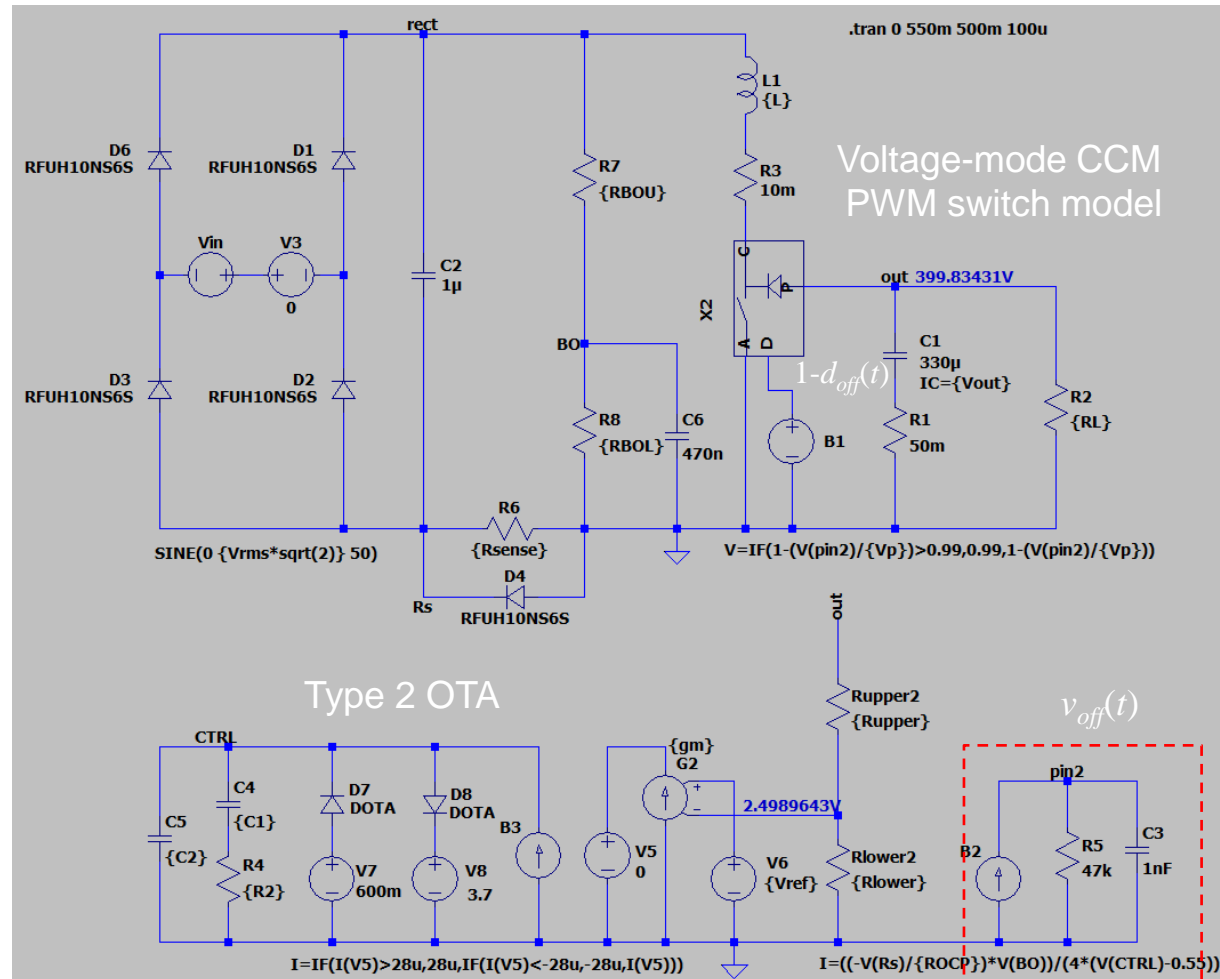
The ramp duration lasts a switching period and is easily determined as:

$T_{sw} = \frac{C_{ramp} V_{ref}}{I_{ch}} \rightarrow I_{ch} = \frac{C_{ramp} V_{ref}}{T_{sw}}$  Replace  $I_{ch}$  in the above expression

$\Rightarrow V_{ref} = V_m + \frac{(C_{ramp} V_{ref} / T_{sw}) dT_{sw}}{C_{ramp}} \rightarrow V_m = V_{ref} (1-d) \Rightarrow R_{in} = \frac{V_{out}}{\langle i_L(t) \rangle} \frac{V_m}{V_{ref}}$

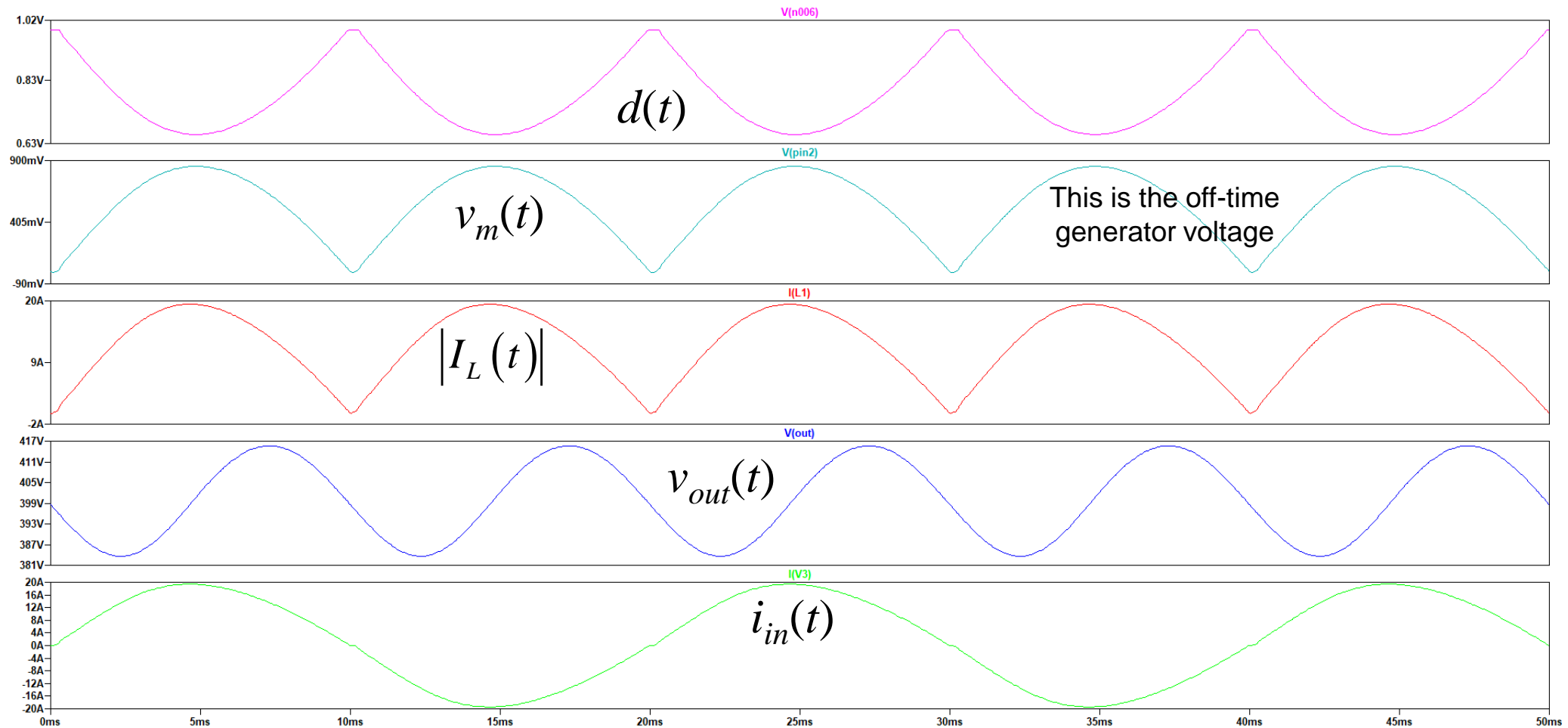
# Averaged Modeling of NCP1654

- The averaged large-signal model will simulate fast in lack of switching component
- SPICE linearizes equations and we can obtain the control-to-output transfer function



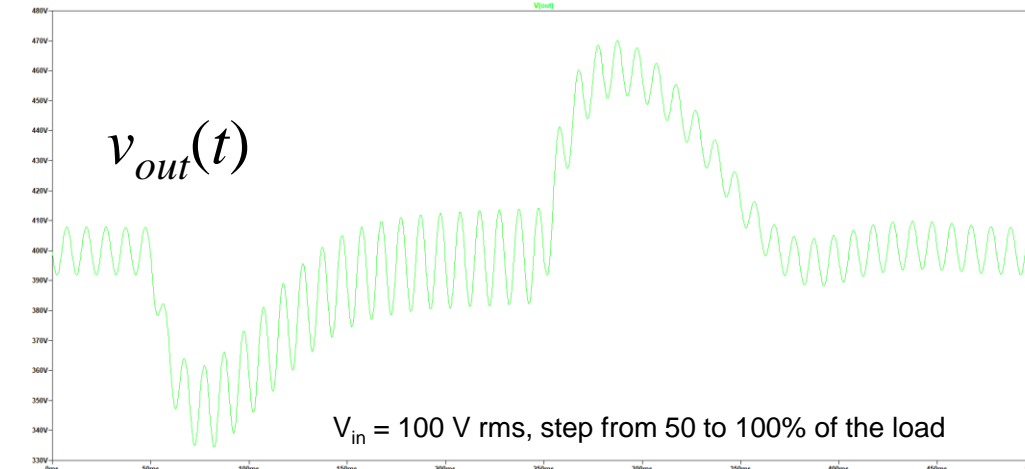
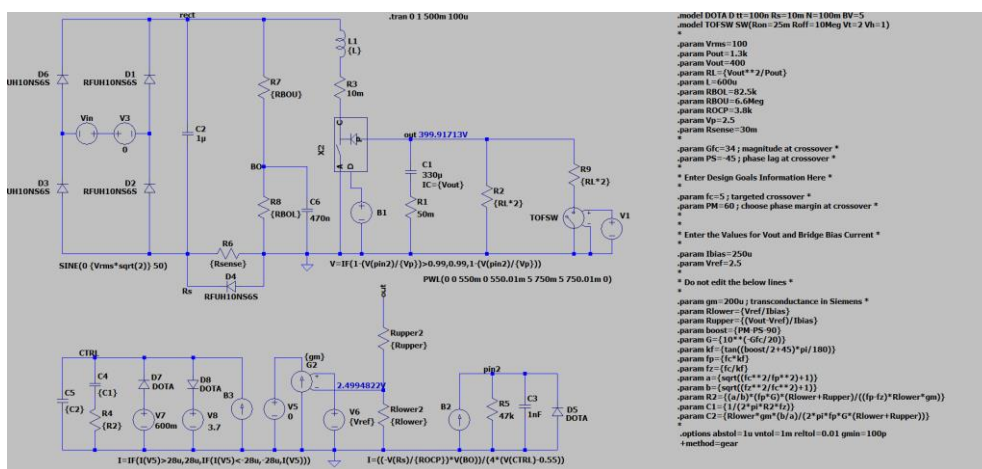
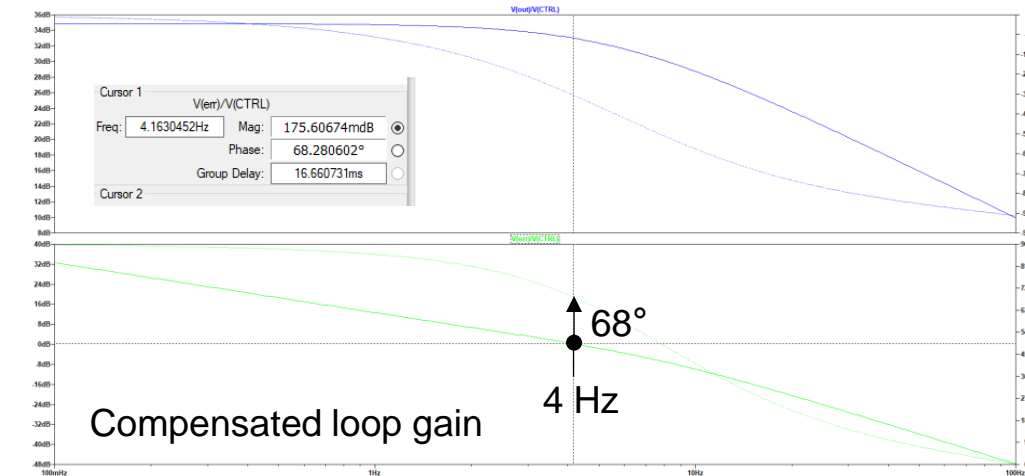
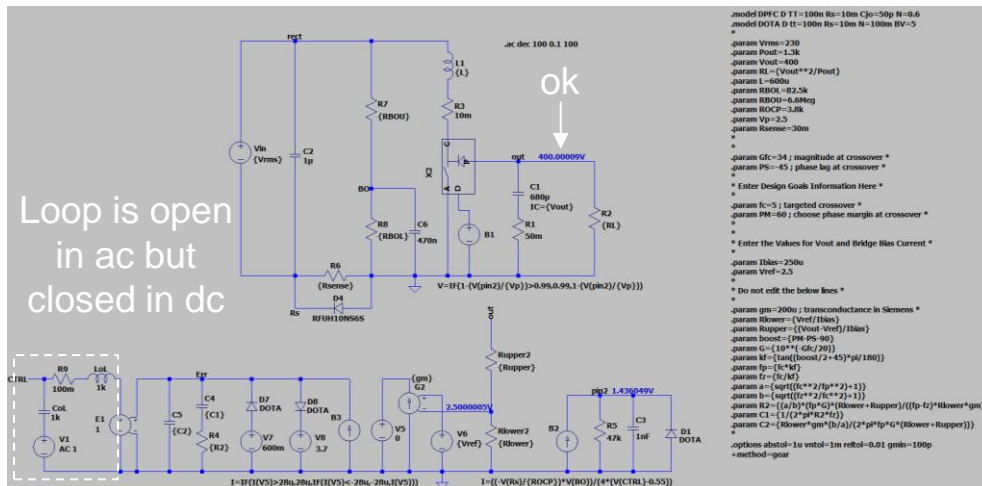
# Simulation Results for the Averaged Model

- The simulation time is extremely fast and helps test the overall architecture
- The low-frequency rms current in the capacitor can be quickly assessed



# Stability Analysis and Compensation

- An averaged model lets you quickly obtain the control-to-output transfer function
- Once in hand, you can think of a compensation strategy and immediately test it

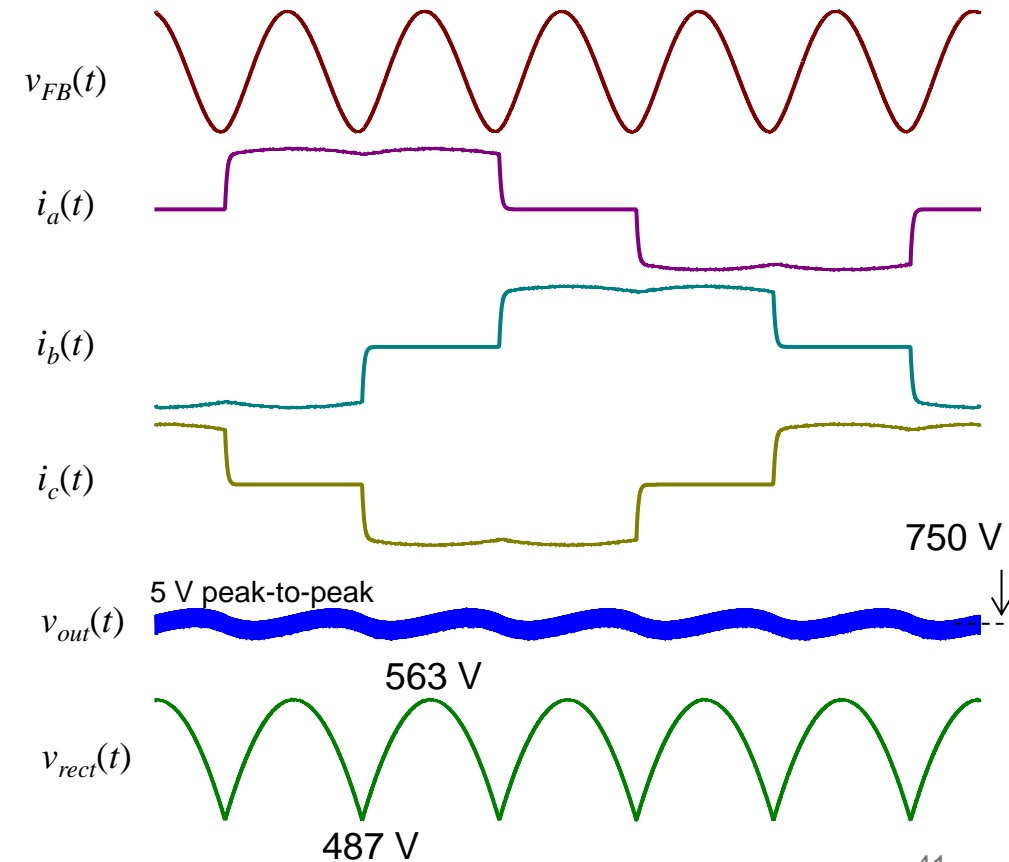
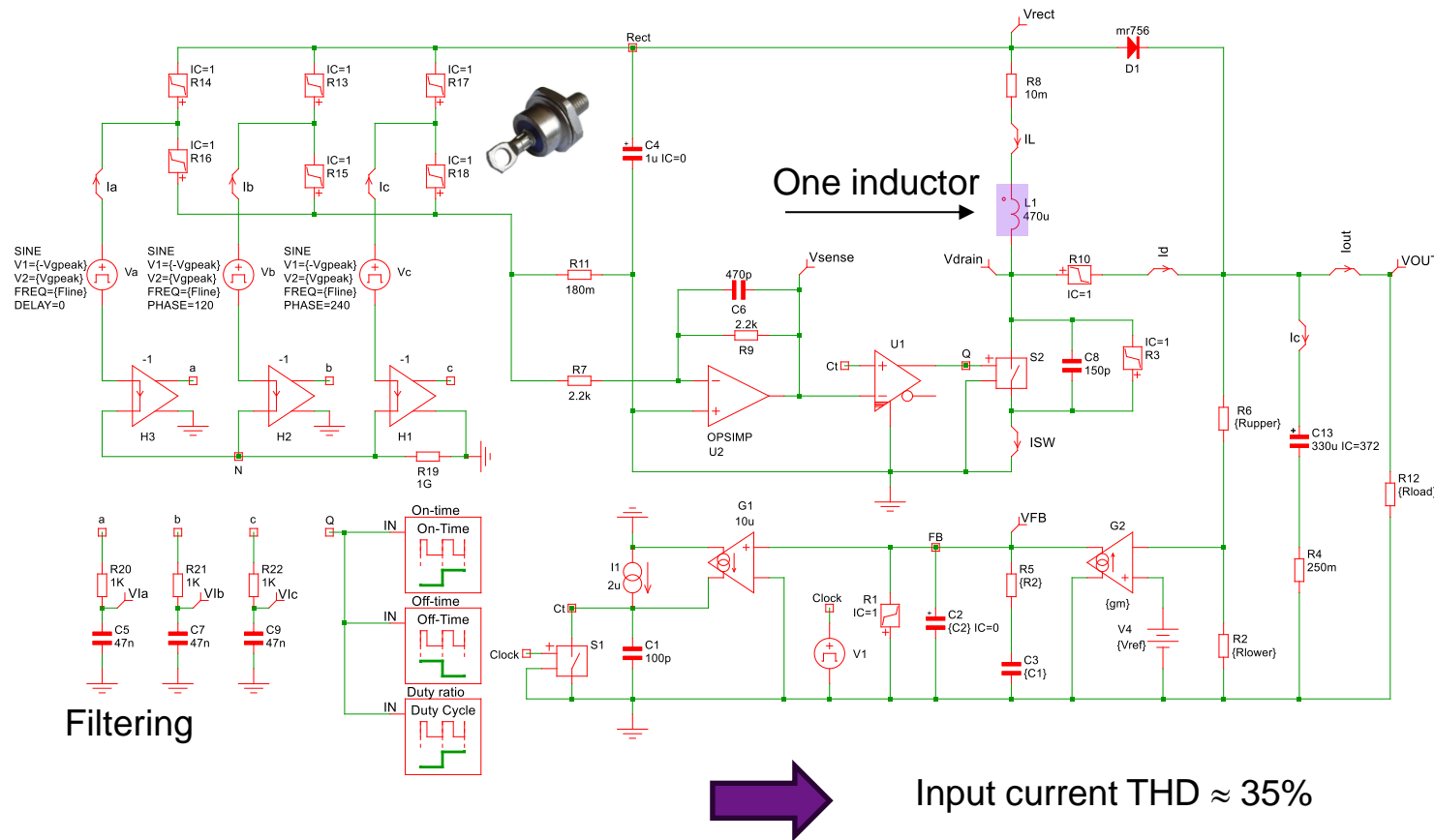


# Agenda

- Notions of Power Factor
- PFC Architectures
- Processing Power – Single Phase
- Processing Power – Three Phases

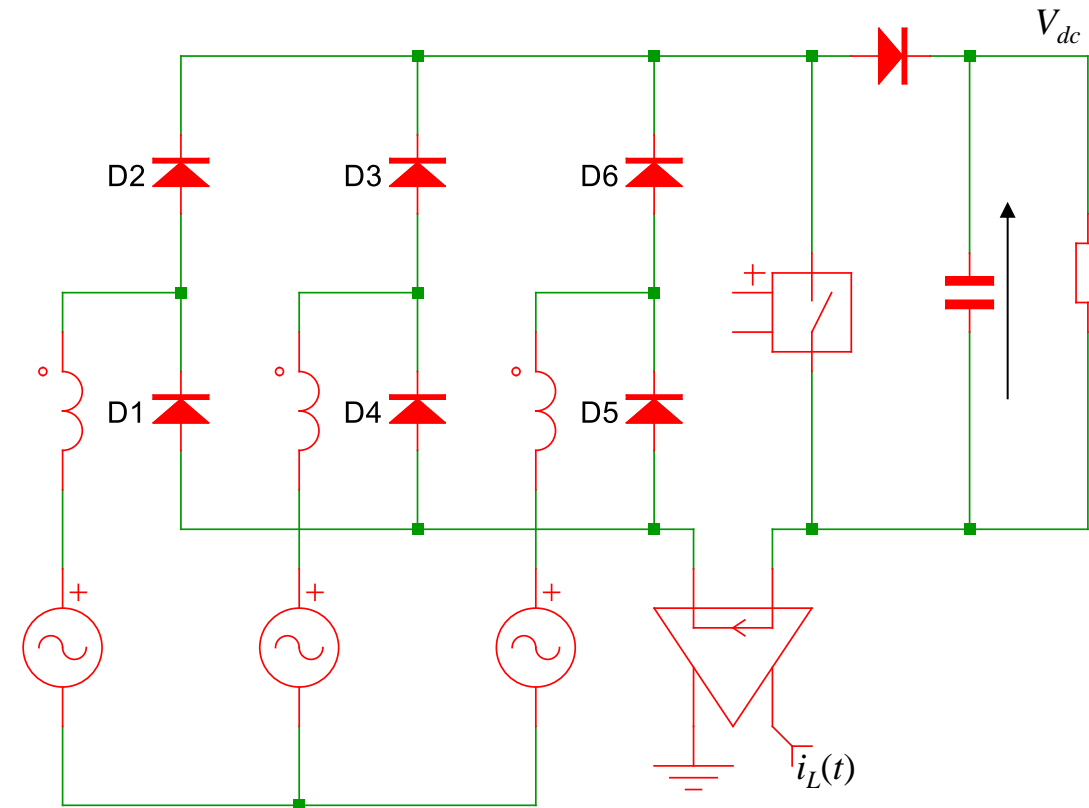
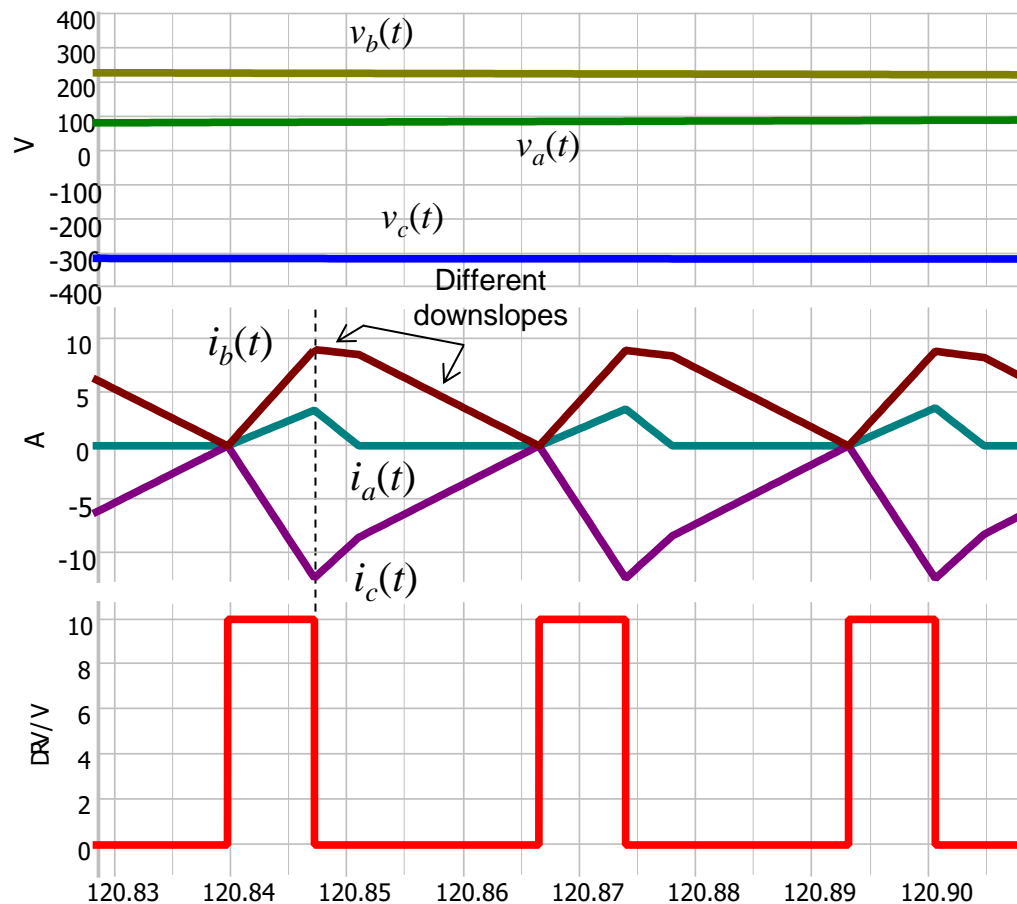
# Three-Phase Single-Switch Active PFC

- The classical boost structure does not lend itself for low-distortion current absorption
- ❖ The input current is distorted considering the “hole” in input diodes conduction time
- ❖ The high-voltage bus is typically regulated at 800 V dc for a 380/480-V ac input



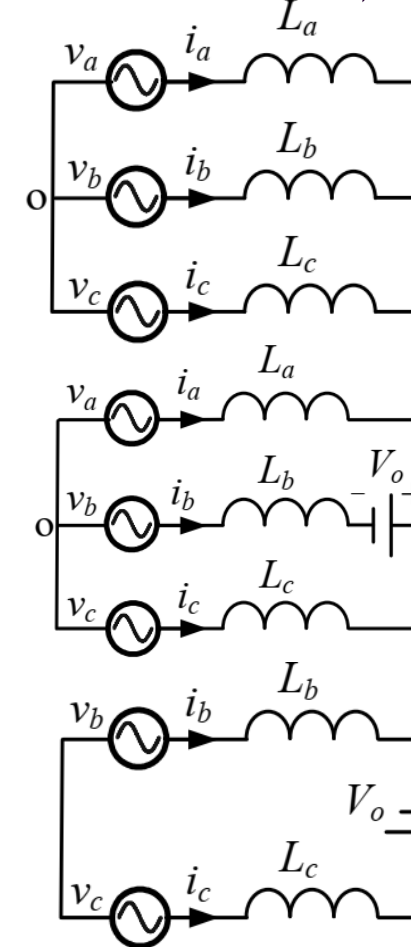
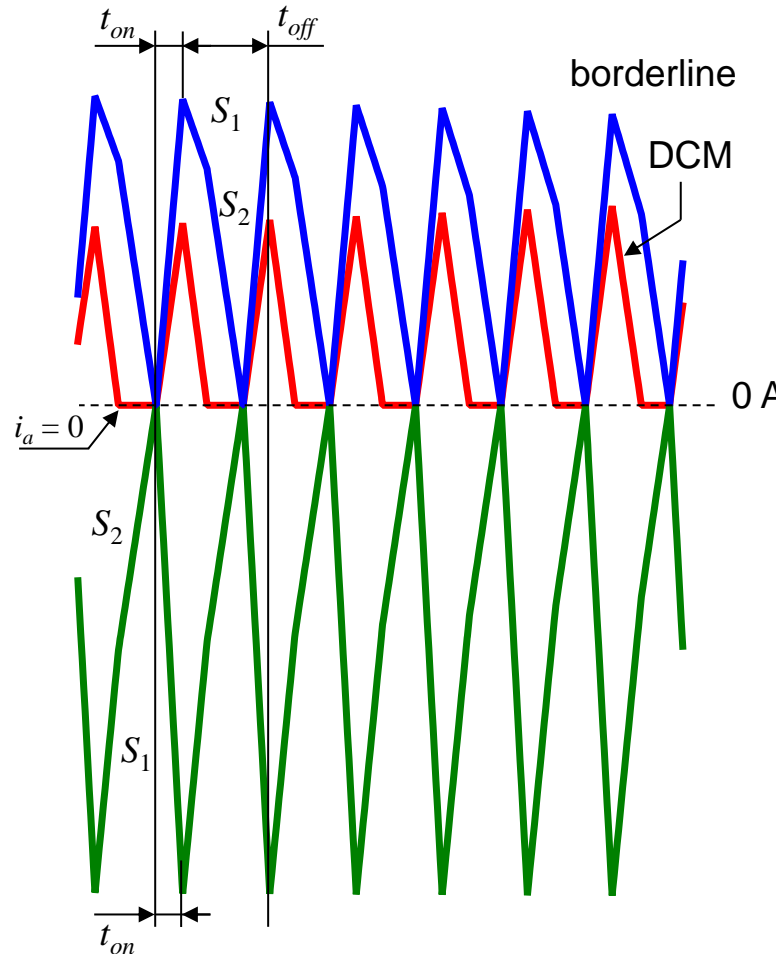
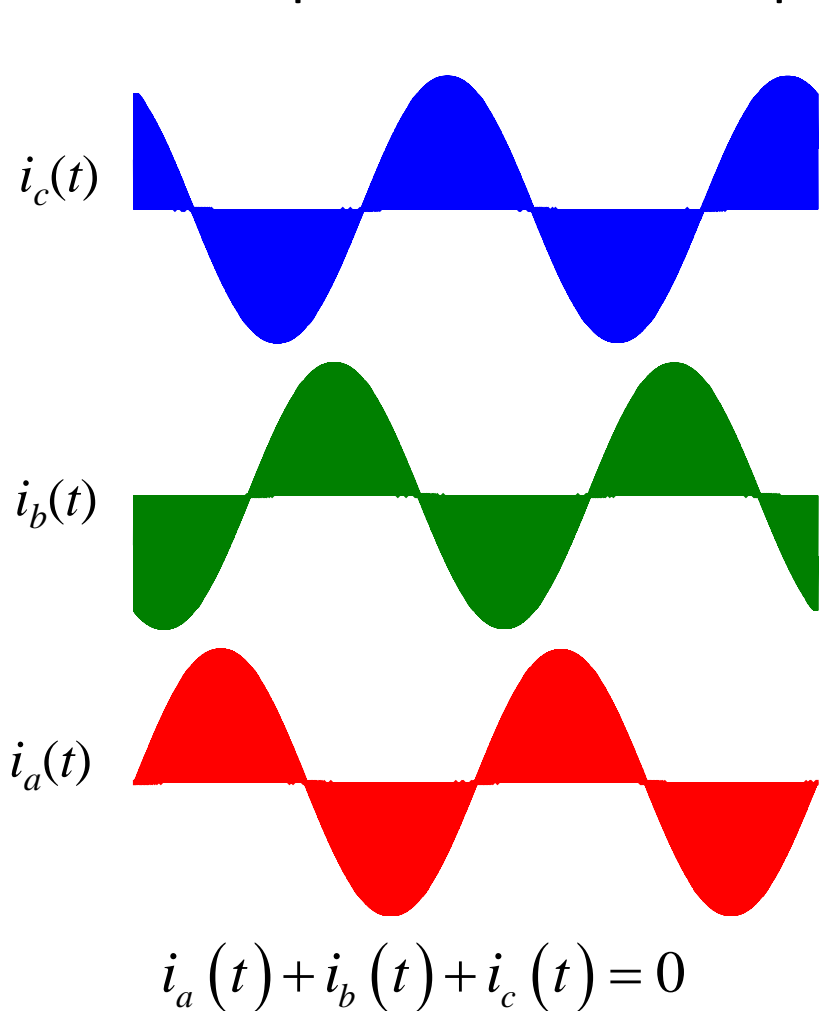
# Single-Switch Borderline Operation

- Rather than using fixed-frequency operation, the PFC operates in borderline operation
- The total inductive current is sensed, ensuring no inductor operates in CCM
- ✓ No particular control law, classical free-running operation, constant on-time



# Non-Sinusoidal Average Inductor Current

- The inductor currents go through different downslopes at the switch turn-off
- The input current envelope is sinusoidal but not the average current  $\Rightarrow \langle i_L(t) \rangle_{T_{sw}} \neq \frac{I_{L,peak}}{2}$



Mains switch is turned on:

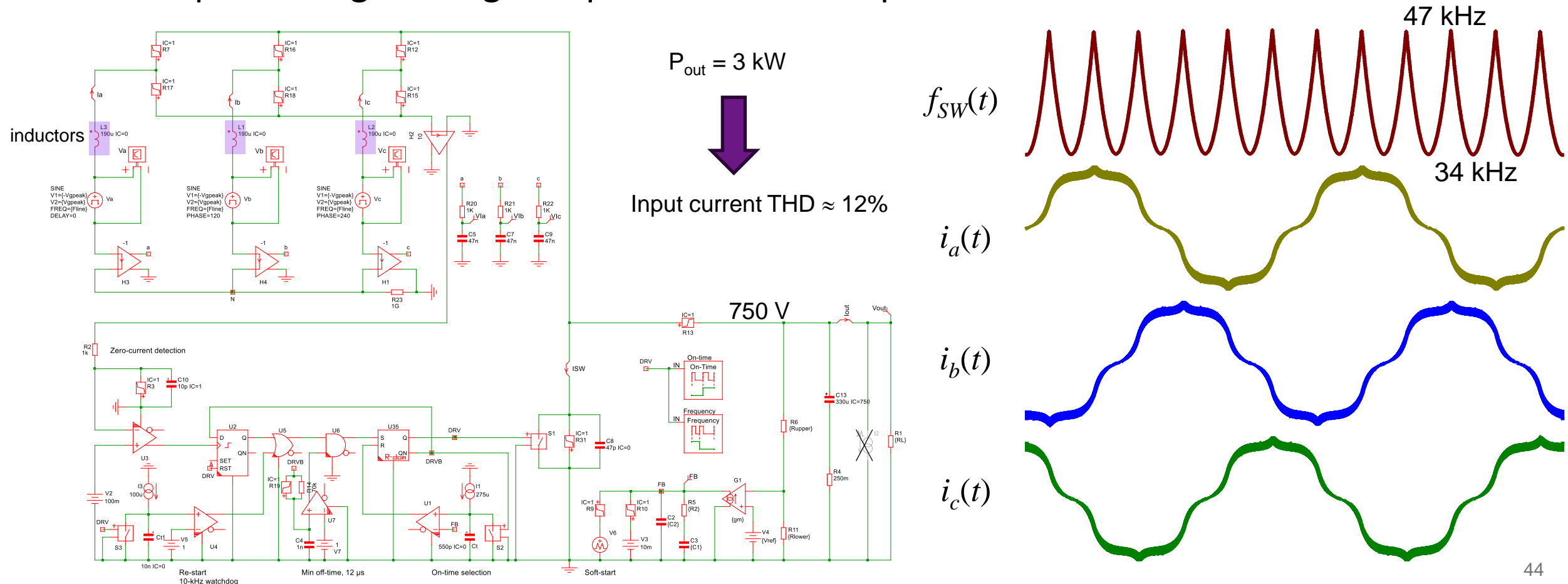
$$S_k = \frac{V_k}{L_k}$$

Mains switch is turned off, diode  $D_b$  conducts

Mains switch is turned off,  $i_a = 0$

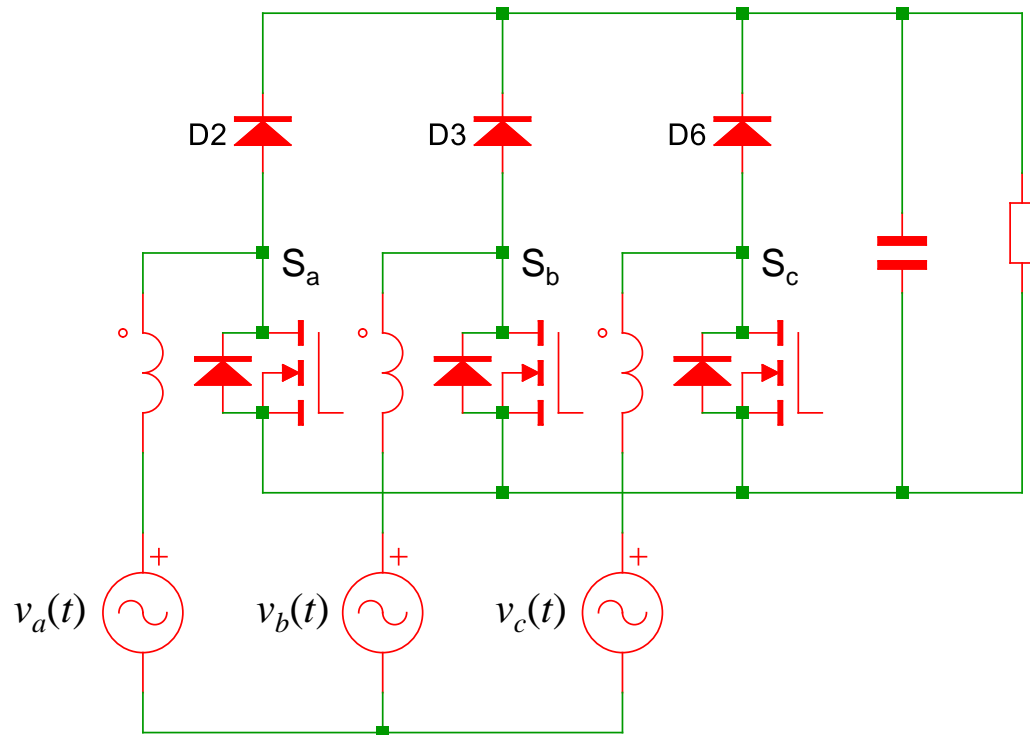
# Simulation of the BCM 3-Phase PFC

- You can implement a BCM circuit where the inductive current is always discontinuous
- ✓ No CCM operation hence lower switching losses at turn-on
- ❖ Requires a high-voltage output to minimize input current distortion

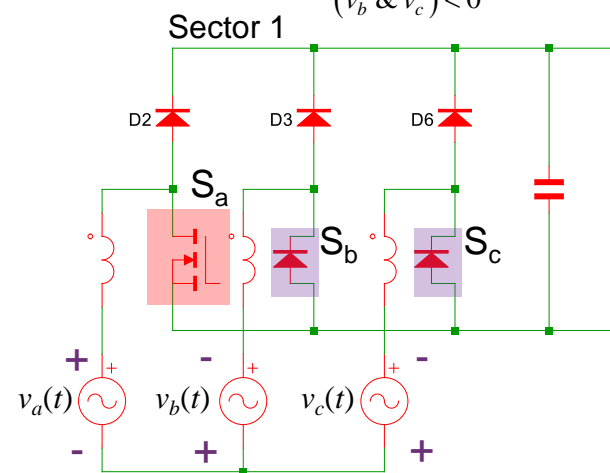
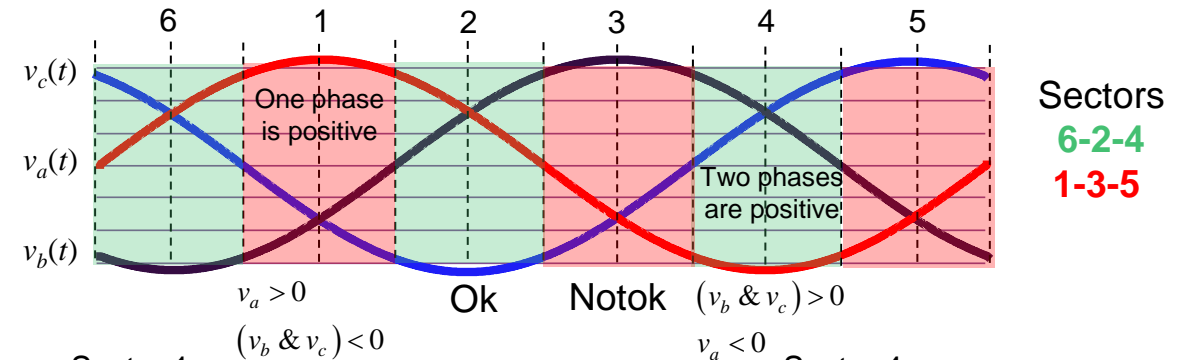


# Three-Phase PFC – Identifying Sectors

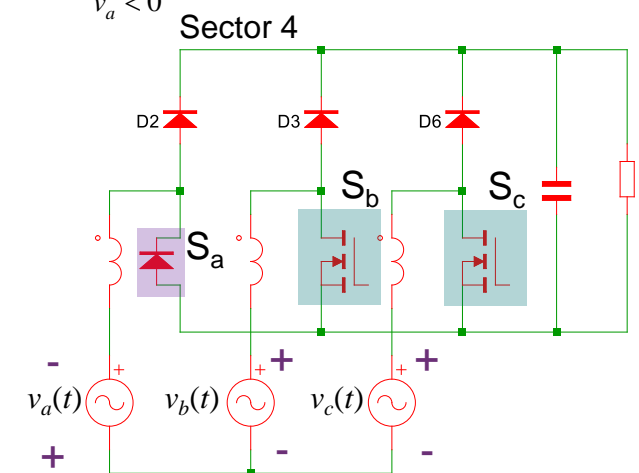
- This hybrid half-controlled 3-switch PFC cannot achieve a sinusoidal input current
- ✓ You can only impress a sinusoidal shape if at least *two* phases are controlled
- ❖ The equation  $i_a(t) + i_b(t) + i_c(t) = 0$  could lead to a sinusoidal input only in a few sectors



J. W. Kolar and T. Friedli, *The Essence of Three-Phase PFC Rectifier Systems—Part I*, *IEEE Transactions on Power Electronics*, vol. 28, no. 1, Jan. 2013



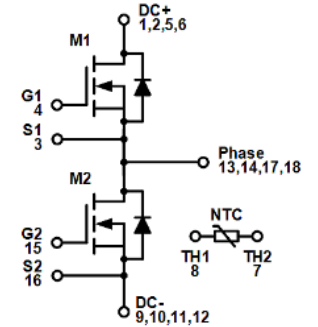
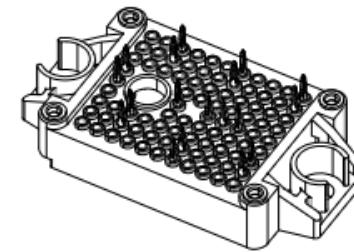
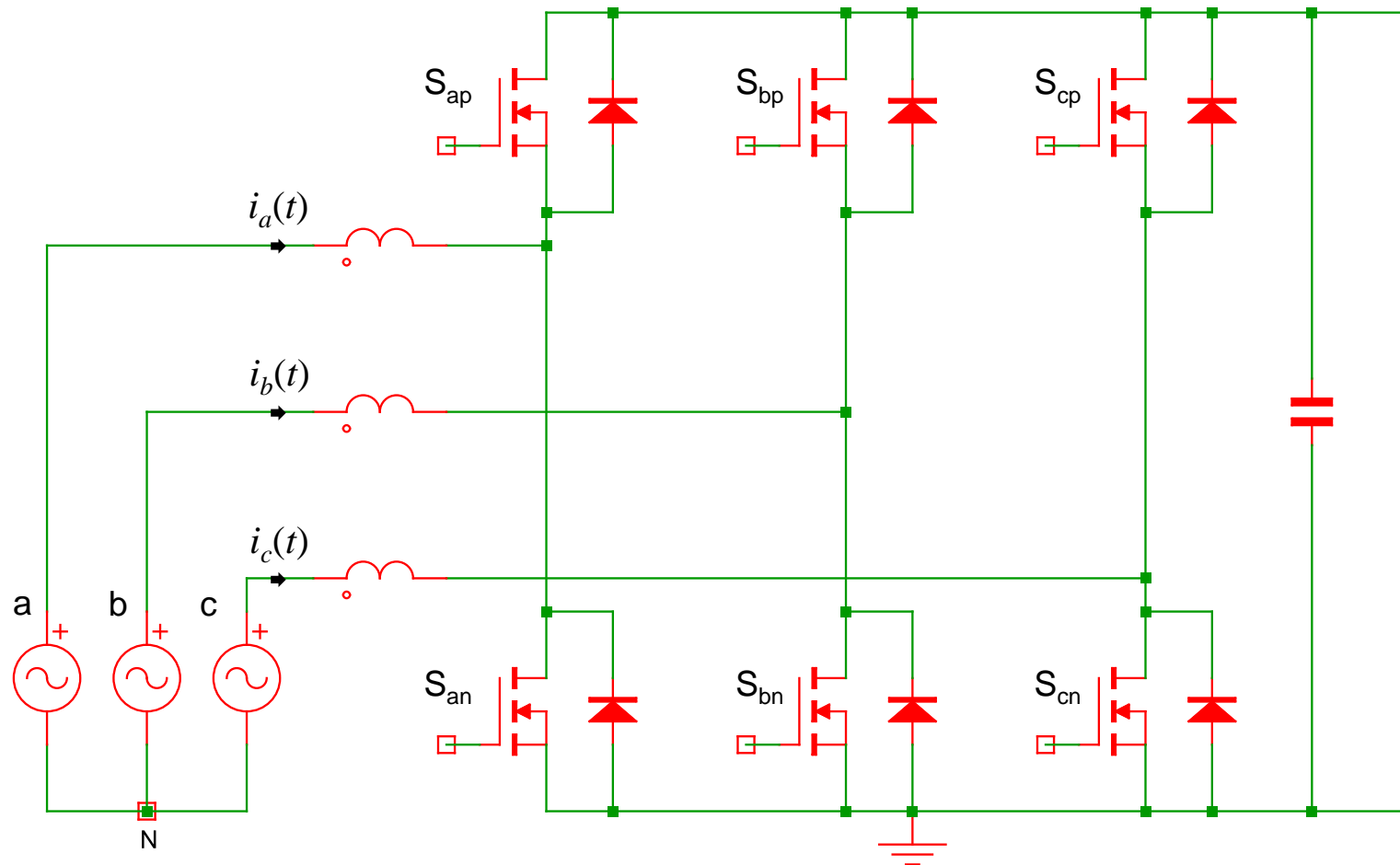
➔  $S_b$  and  $S_c$  switches have no effect as body diodes conduct



➔  $S_b$  and  $S_c$  are driven,  $S_a$  body conducts:  $i_a = -(i_b + i_c)$

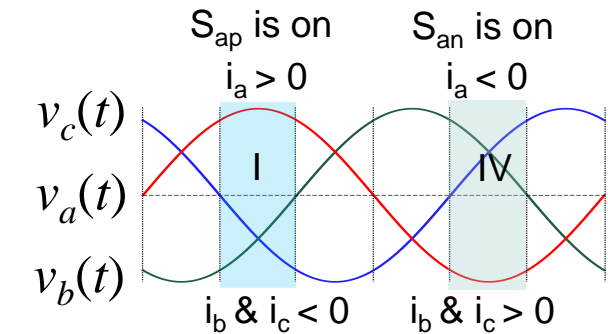
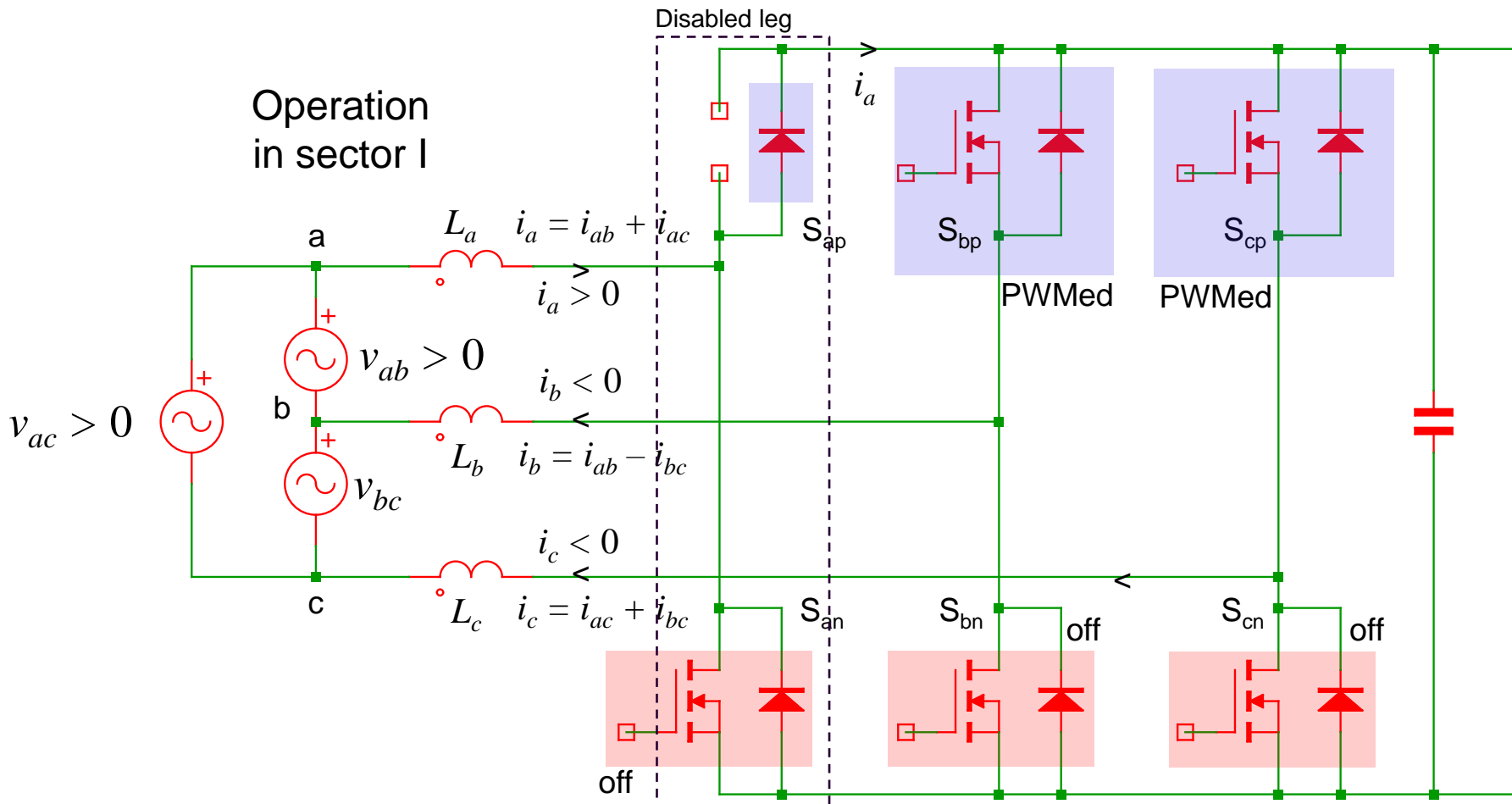
# Six-Switch or Sixpack Configuration

- This is a 2-level bidirectional boost converter allowing sinusoidal current absorption
- Several techniques exist to control the power switches like 6-step modulation and dq0



# 6-Step Operation Needs Logic Decoding

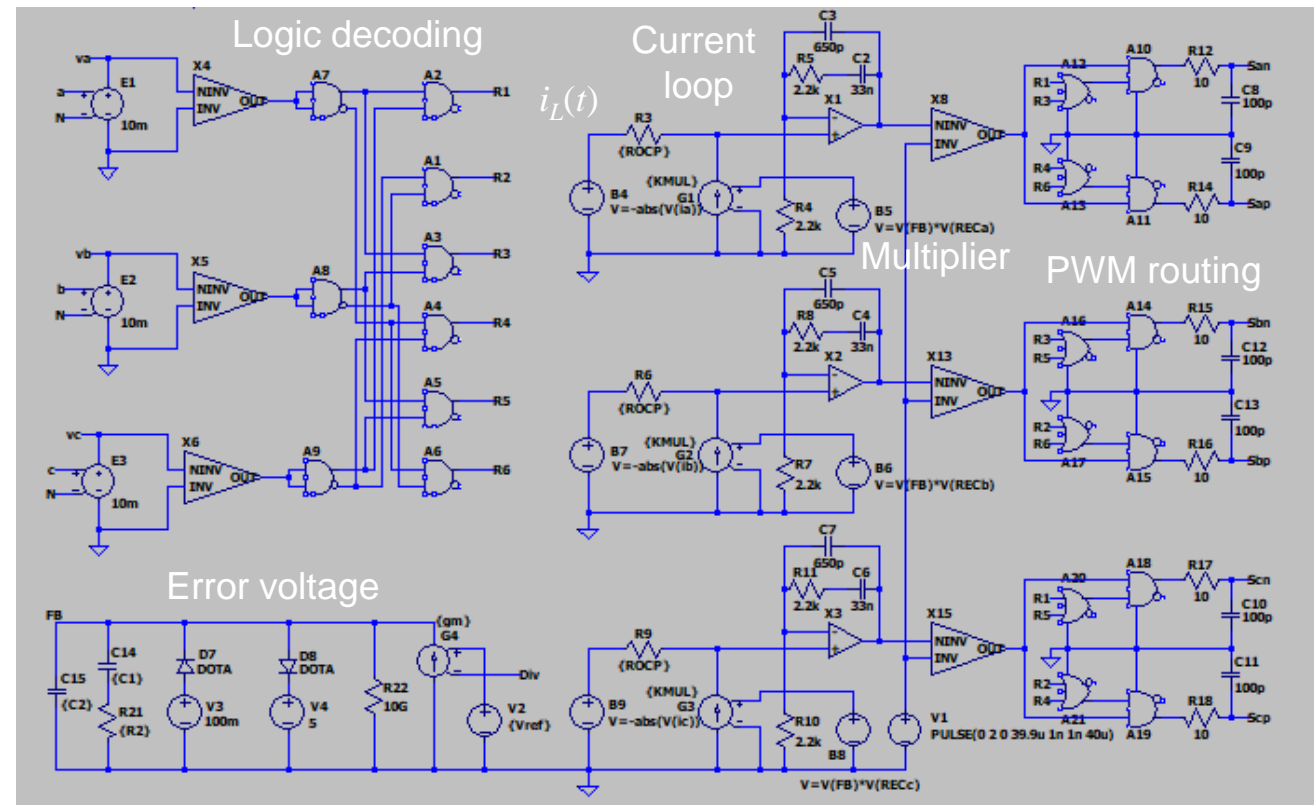
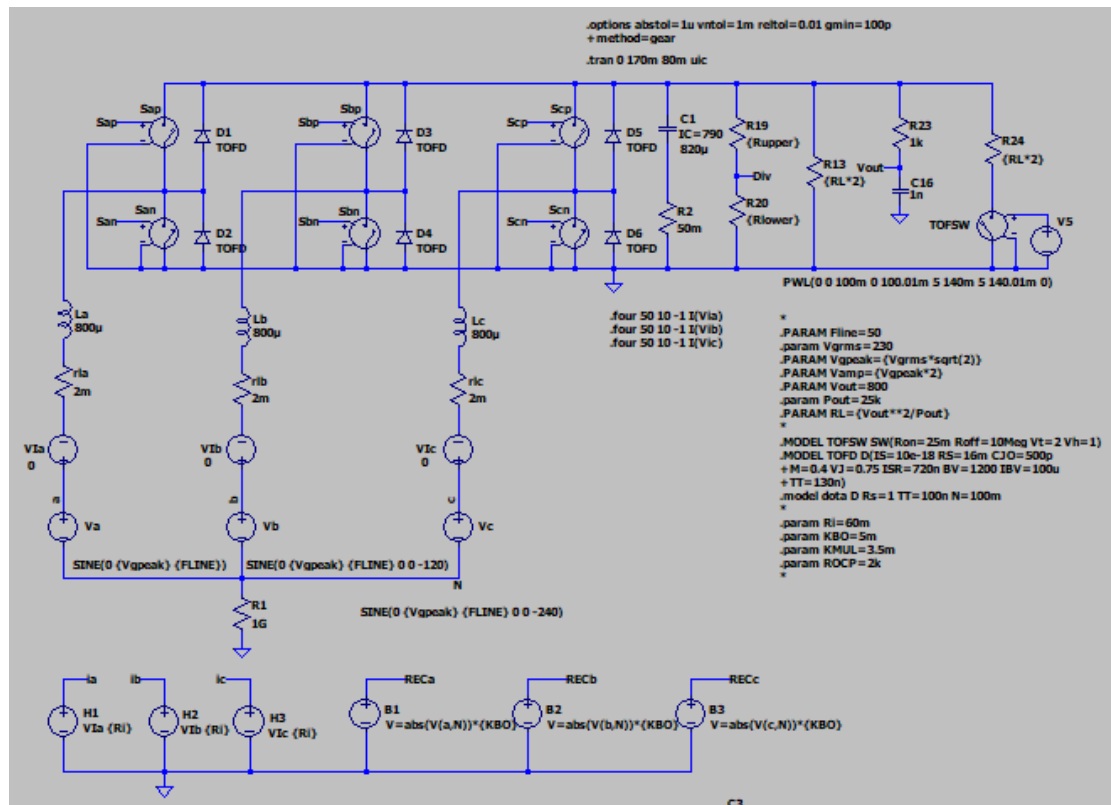
- You cannot impress a sinusoidal shape to phase A in sector 1 as  $S_{ap}$  conducts
- Two legs are made active while one of them is kept passive



- ✓  $S_{ap}$  is on permanently in sector I –  $S_{bp}$  &  $S_{cp}$  PWMed
- ✓  $S_{an}$  is on permanently in sector IV –  $S_{bn}$  &  $S_{cn}$  PWMed
- Leg A is off in sectors I and IV
- Leg B is off in sectors III and VI
- Leg C is off in sectors II and V

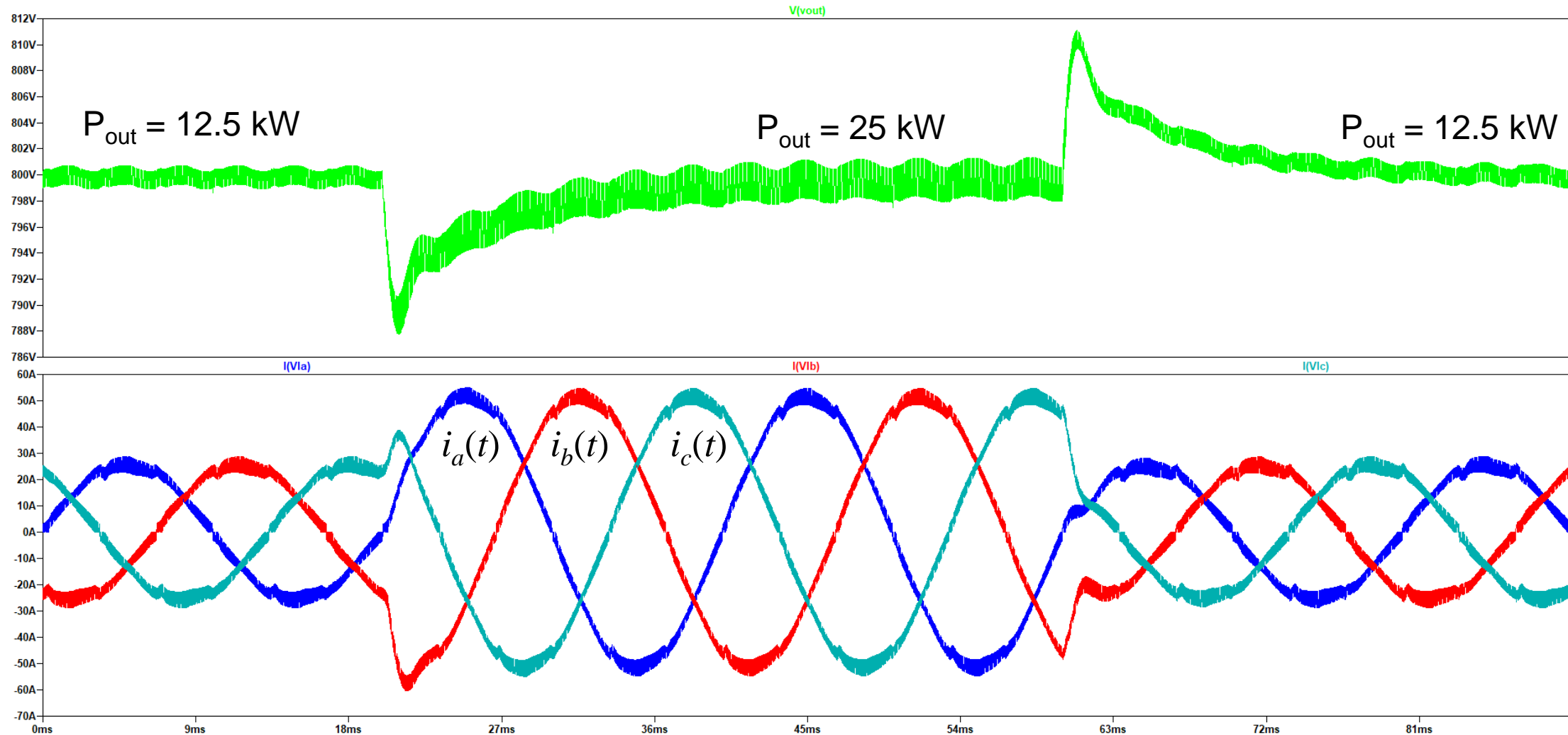
# Six-Pack Simulation with LTspice

- The PFC is supplied from a 400-V phase-to-phase level and delivers 800 V/25 kW
- The switching frequency is 25 kHz – the loop has been compensated with SIMPLIS
- Three multipliers are used to shape the inductor current envelope



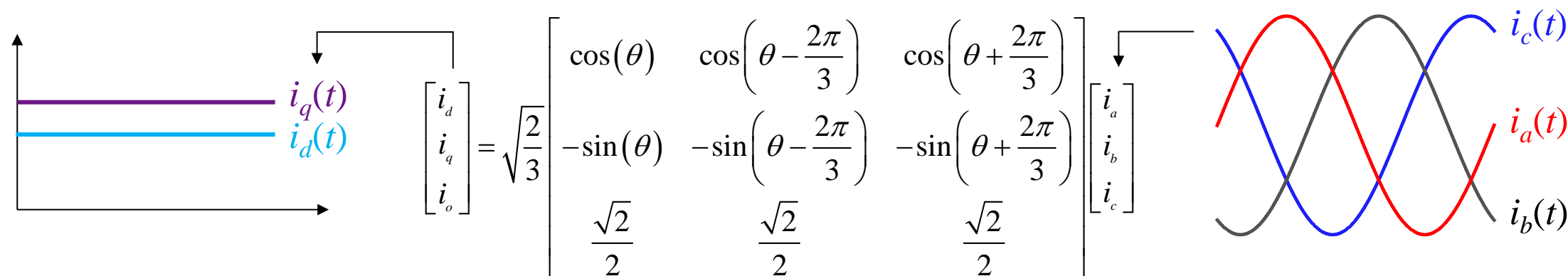
# Testing the Transient Response

- The transient response from 50% to 100% of nominal power is excellent

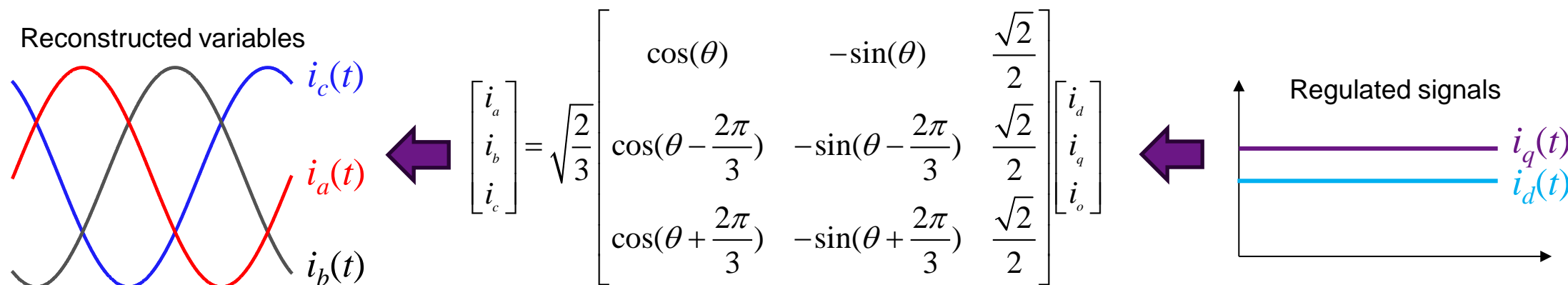


# The dq0 Transformation

- We have three sinusoidal voltage sources and we want a resistive input
- We can transform the 3-variable input into two dc components, d and q
- Perform regulation on d and q and convert back into three sinusoidal setpoints

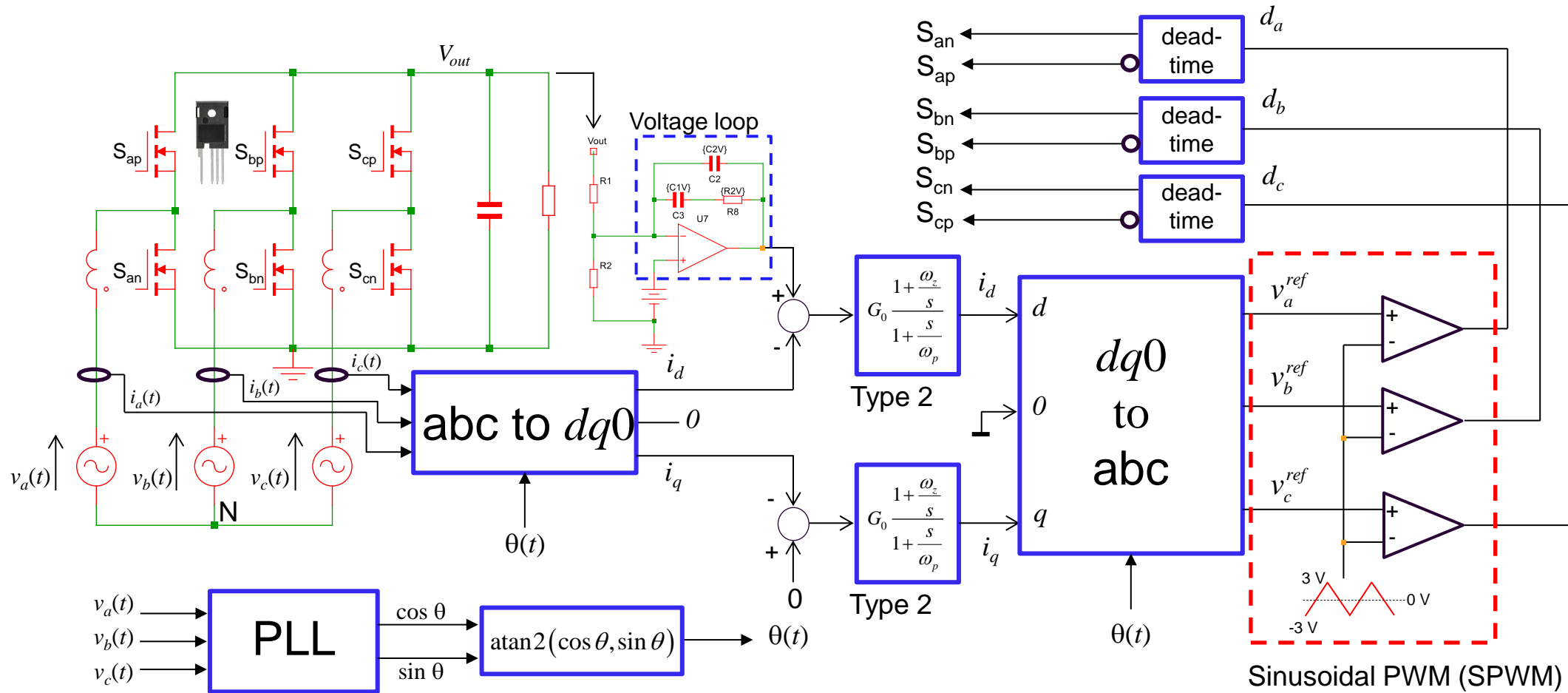


✓ The inverse  $dq0$  reconstructs the corrected waveforms after corrected  $d$  and  $q$  variables



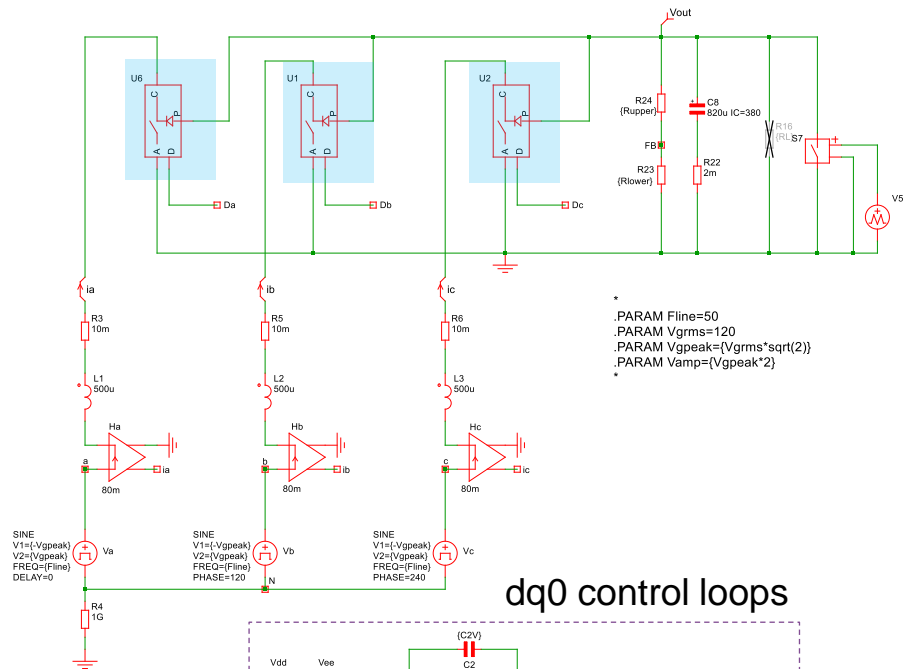
# Three-Phase Rectifier with SPWM

- A phase-locked loop (PLL) is used for extracting the angle  $\theta$
- Each input current is sensed and used to compute  $dq0$  variables with  $\theta$

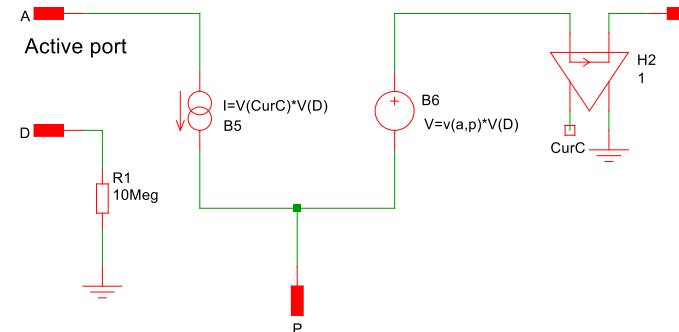


# Average Modeling of the Whole Chain

- The PWM switch model lends itself perfectly for this 3-phase PFC ac simulation



.PARAM Fline=50  
.PARAM Vgrms=120  
.PARAM Vgpeak={Vgrms\*sqrt(2)}  
.PARAM Vamp={Vgpeak\*2}



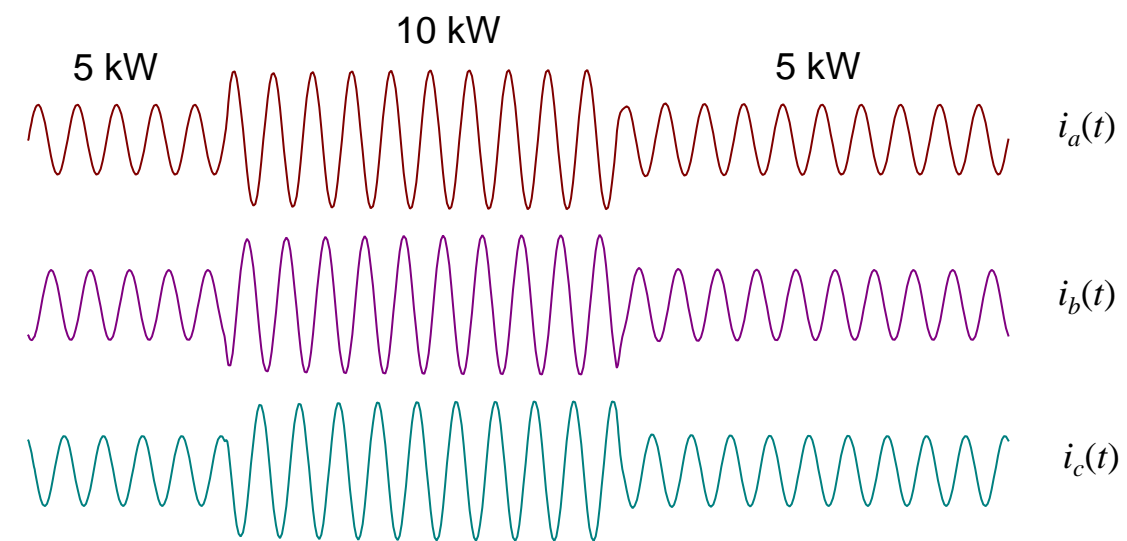
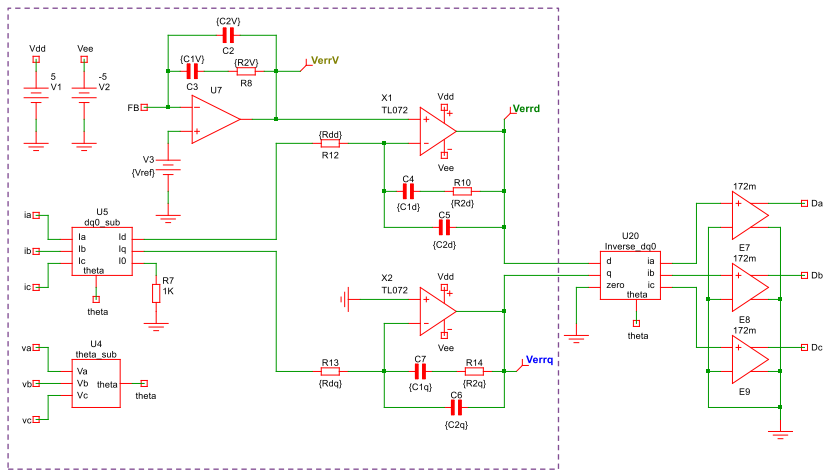
Simplified Analysis of PWM Converters Using Model of PWM Switch  
Part I: Continuous Conduction Mode

VATCHÉ VORPÉRIAN  
Virginia Polytechnic Institute and State University

V. Vorpérian, *Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode*, in *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, no. 3., May 1990

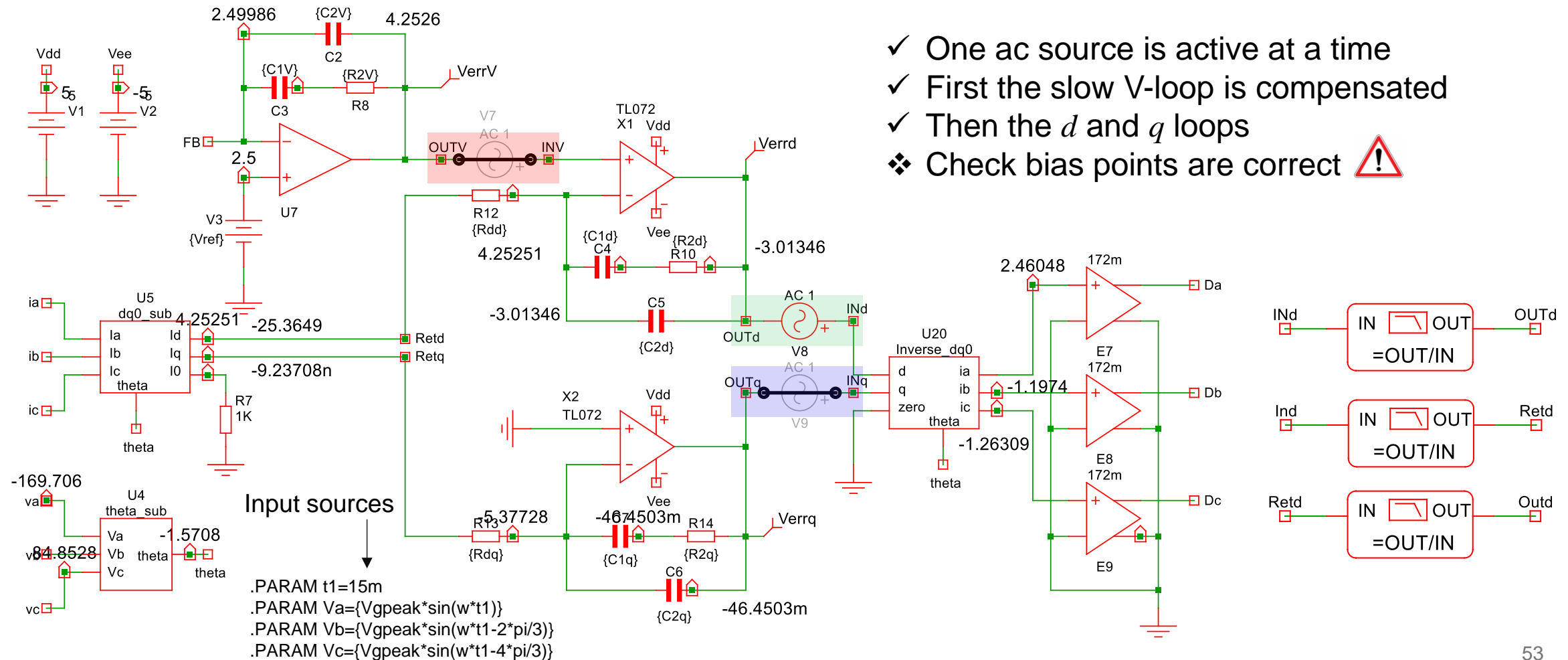
- I have replaced the switching cell by the VM PWM switch model
  - Pulse-width modulators are replaced by small-signal gains

## dq0 control loops

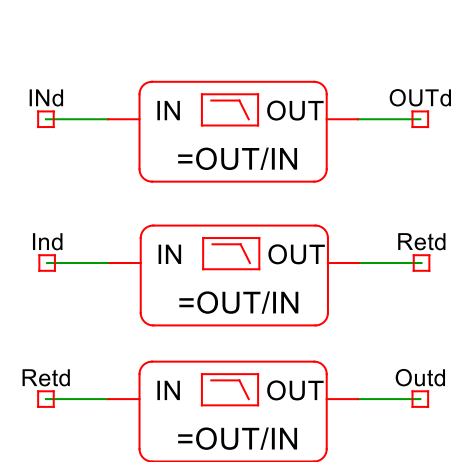


# Three Loops have to be Compensated

- Three loops:  $V_{out}$  to be regulated at 400 V and the  $d$  and  $q$  paths
- The voltage loop will be closed with a 20-Hz crossover while  $f_c$  for  $d$  and  $q$  will be 2 kHz

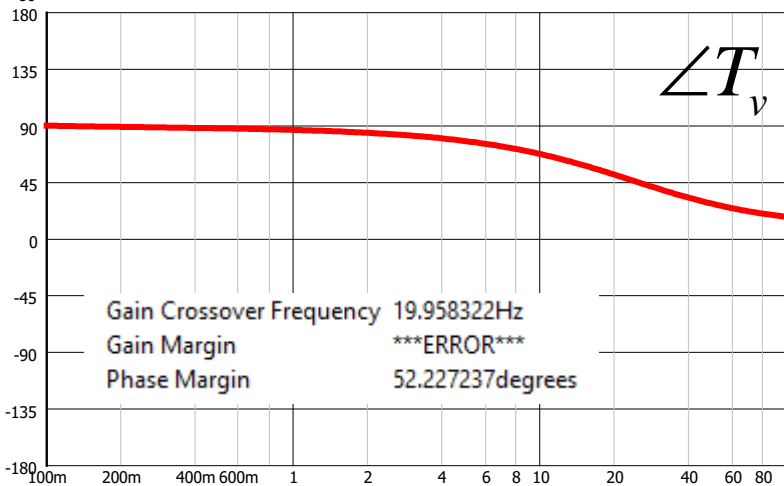


- ✓ One ac source is active at a time
- ✓ First the slow V-loop is compensated
- ✓ Then the  $d$  and  $q$  loops
- ❖ Check bias points are correct

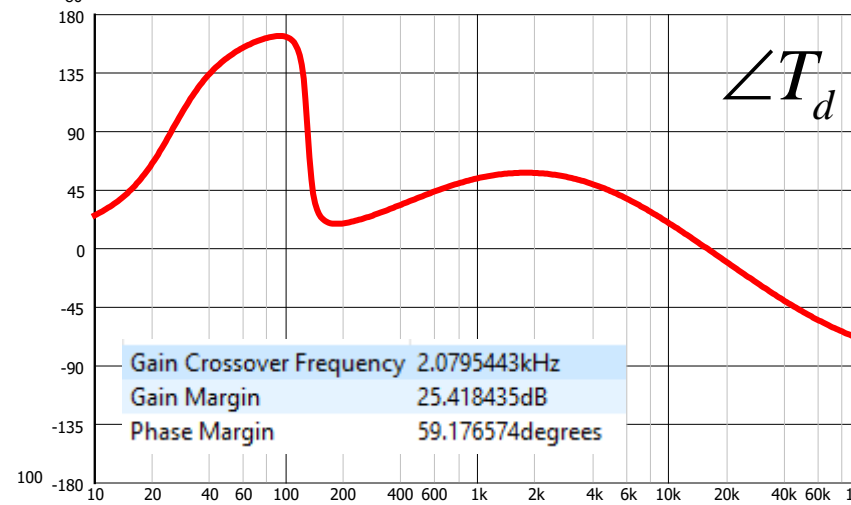
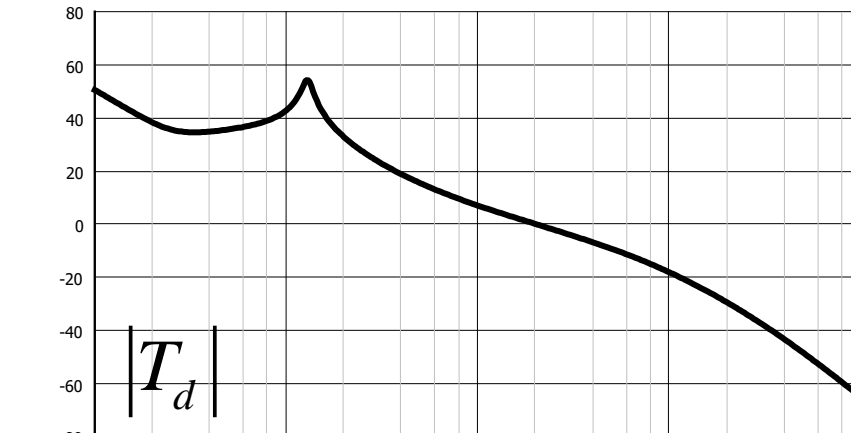


# All Loops show Comfortable Margins

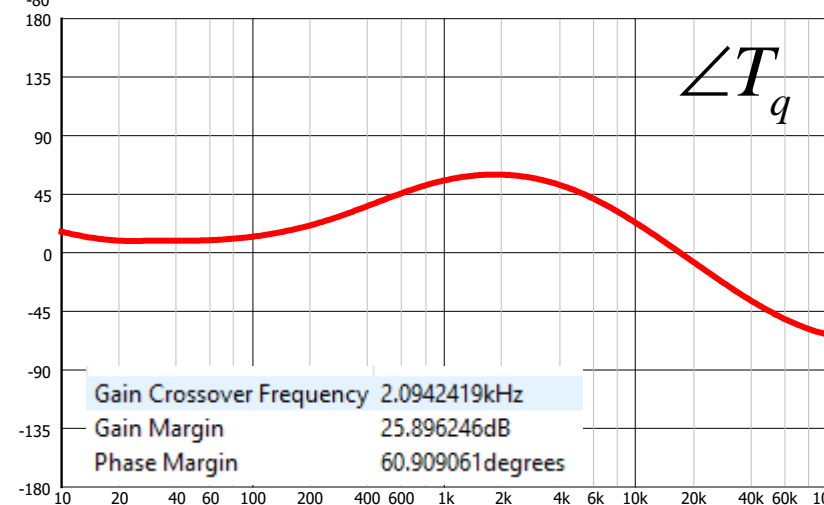
- The three loops are individually compensated with adequate phase and gain margins



Voltage loop –  $f_c = 20$  Hz



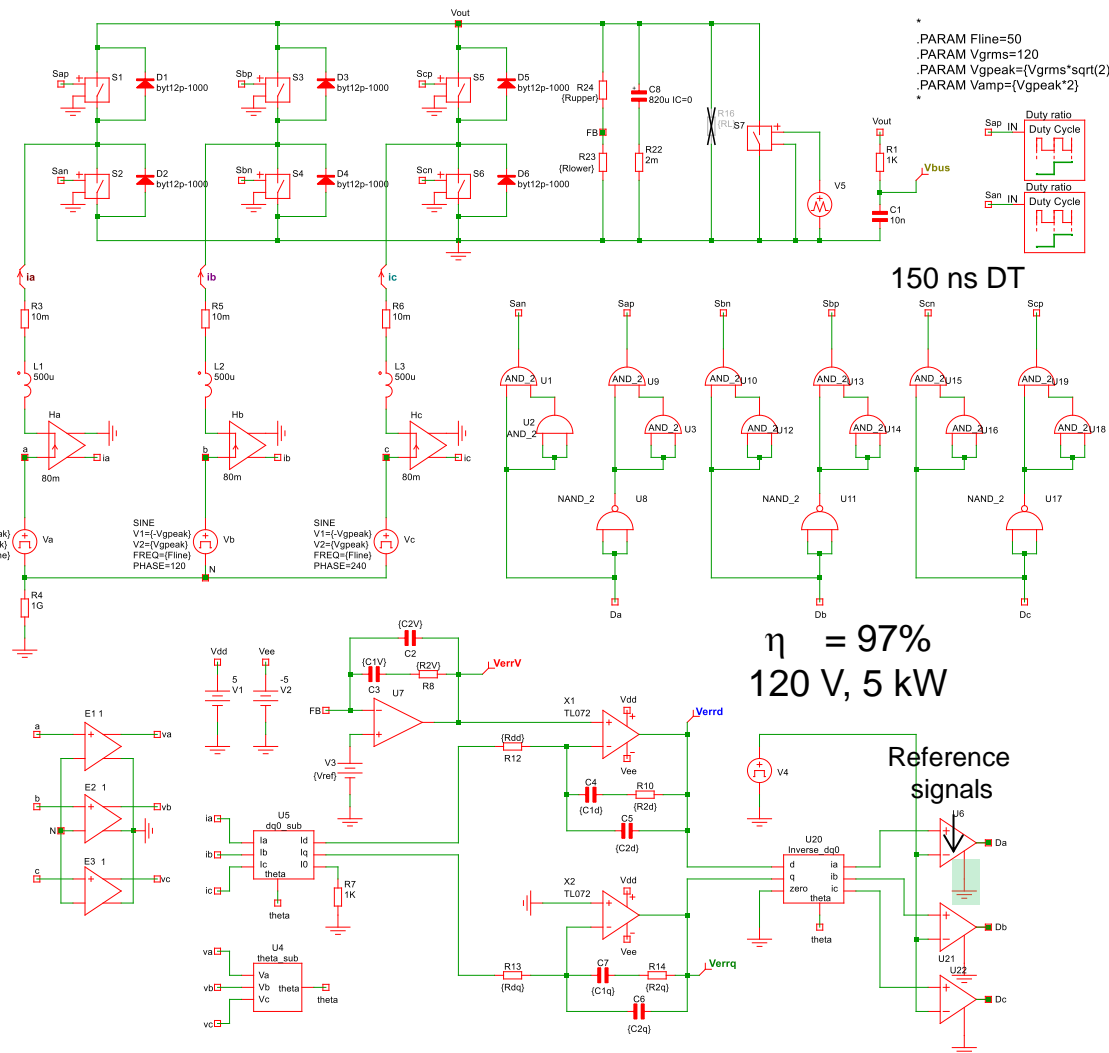
d loop –  $f_c = 2$  kHz



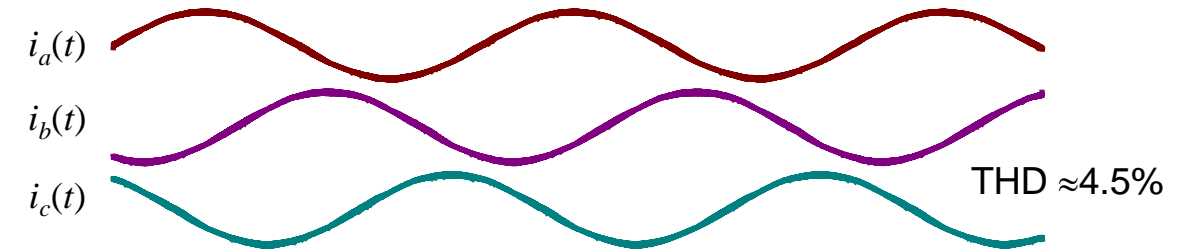
q loop –  $f_c = 2$  kHz

# Cycle-by-Cycle Simulation with SIMetrix

- This cycle-by-cycle SIMetrix simulation is fast and gives results in less than 5 mn



- There are three compensators in this circuit
- The voltage loop is compensated for a low crossover
- The inner current loops are faster  $\approx 1-2$  kHz
- The converter delivers 5 kW from a 120-V ac input



.param GfcV=20 ; magnitude at crossover \*  
 .param PSV=-90 ; phase lag at crossover \*  
 \*

\* Enter Design Goals Information Here \*

.param fcV=20 ; targeted crossover \*  
 .param PMV=60 ; choose phase margin at crossover \*  
 \*

\* Enter the Values for Vout and Bridge Bias Current \*  
 \*

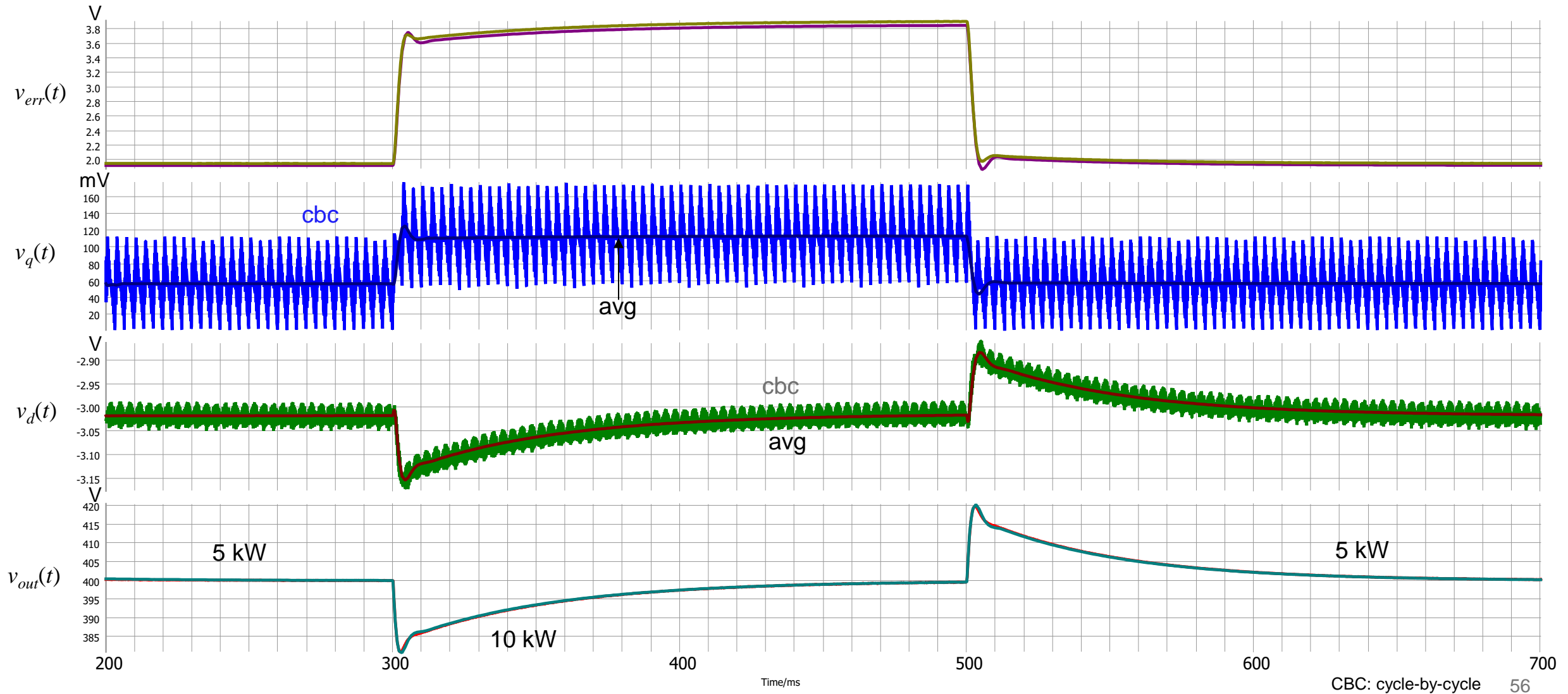
.param Vout=400  
 .param Pout=5k  
 .param RL={{(Vout)^2/(Pout)}}  
 .param Ibias=100u  
 .param Vref=2.5  
 .param Rlower={{Vref/Ibias}}  
 .param Rupper={{(Vout-Vref)/Ibias}}

\* Do not edit the below lines \*  
 .param boostV={{PMd-PSd-90}}  
 .param GV={{10^(-GfcV/20)}}  
 .param kV={{tan((boostV/2+45)\*pi/180)}}  
 .param fpV={{fcV\*kV}}  
 .param fzV={{fcV/kV}}  
 .param C2V={{1/(2\*pi\*fcV\*GV\*kV\*Rupper)}}  
 .param C1V={{C2V\*(kV^2-1)}}  
 .param R2V={{kV/(C1V\*2\*pi\*fcV)}}  
 \*

Type 2 voltage loop  
compensation

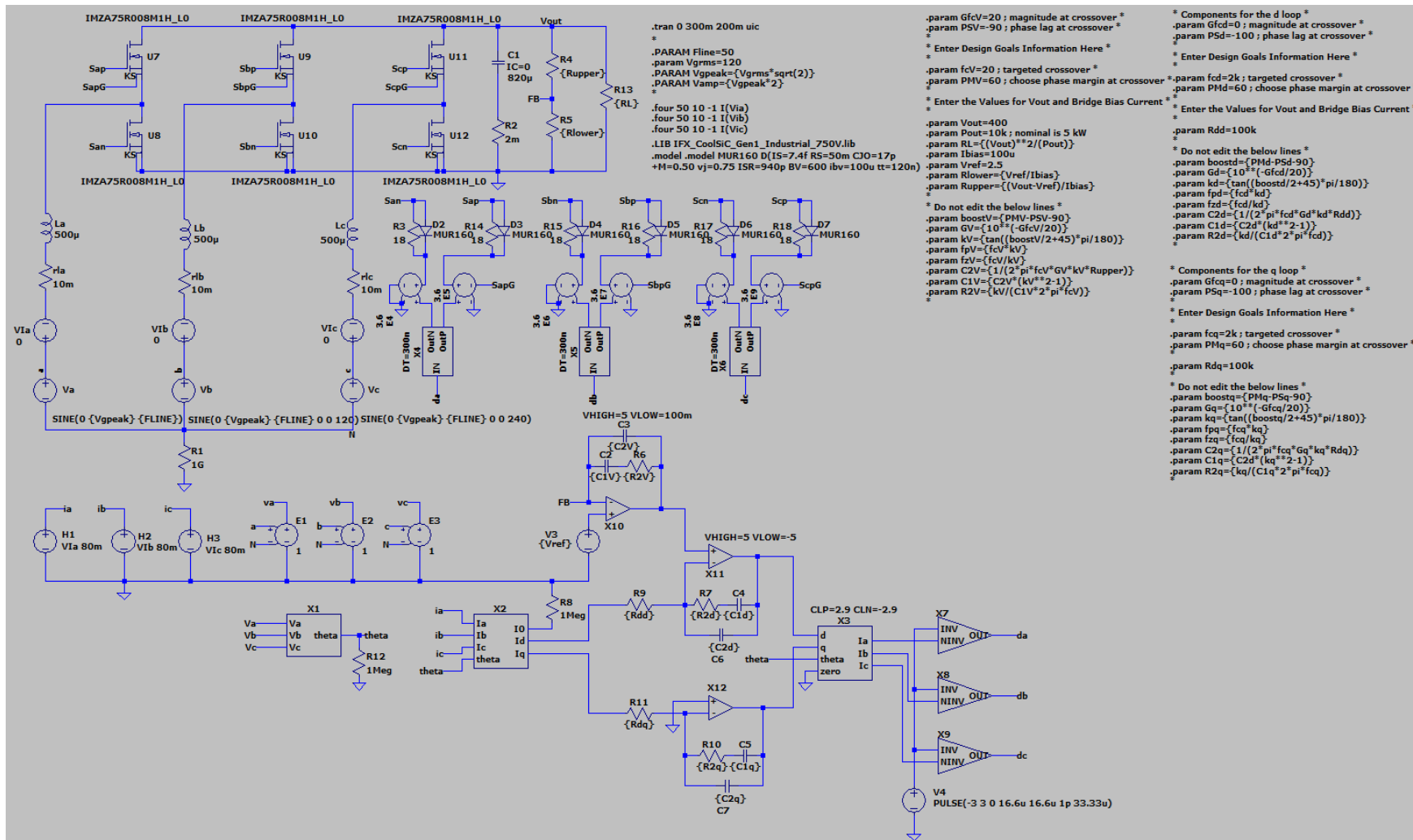
# Now compare Averaged and CBC Models

- Excellent correlation between cycle-by-cycle and average model waveforms

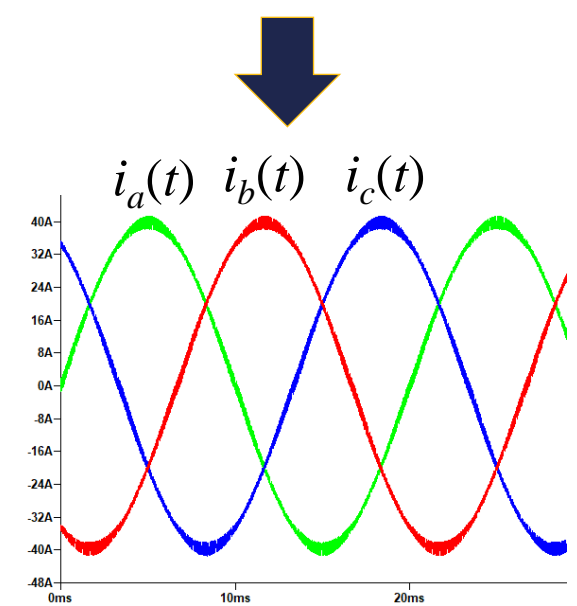


# Simulation was also performed in LTspice

- LTspice can also run the entire simulation with SiC transistor models

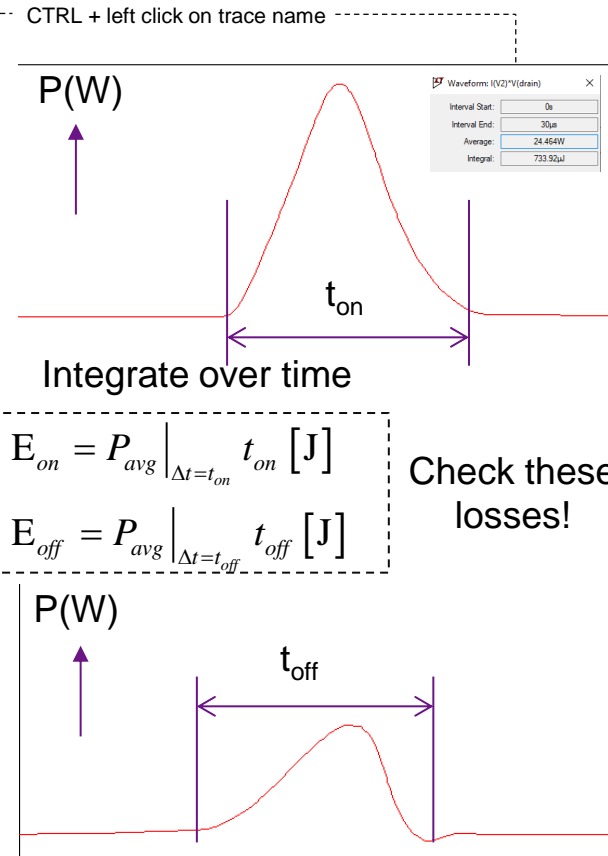
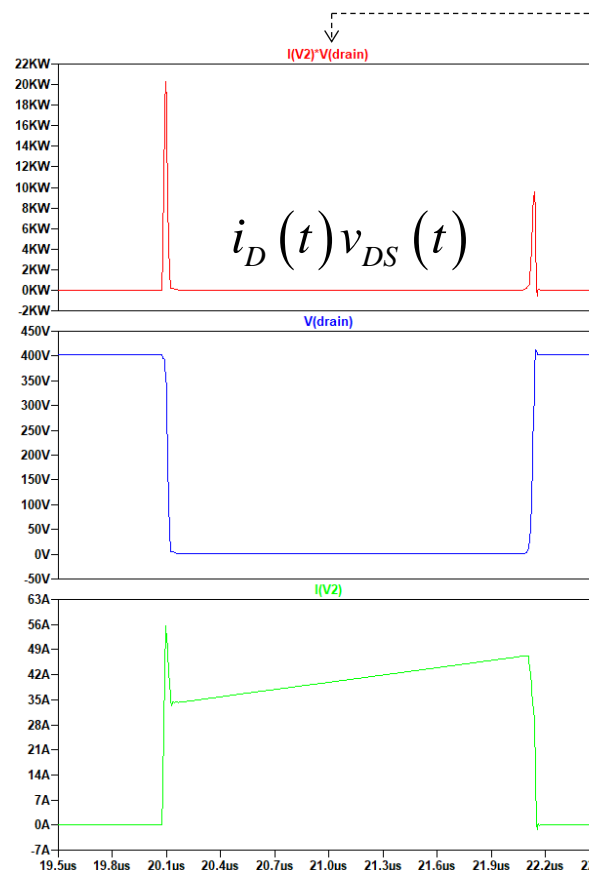
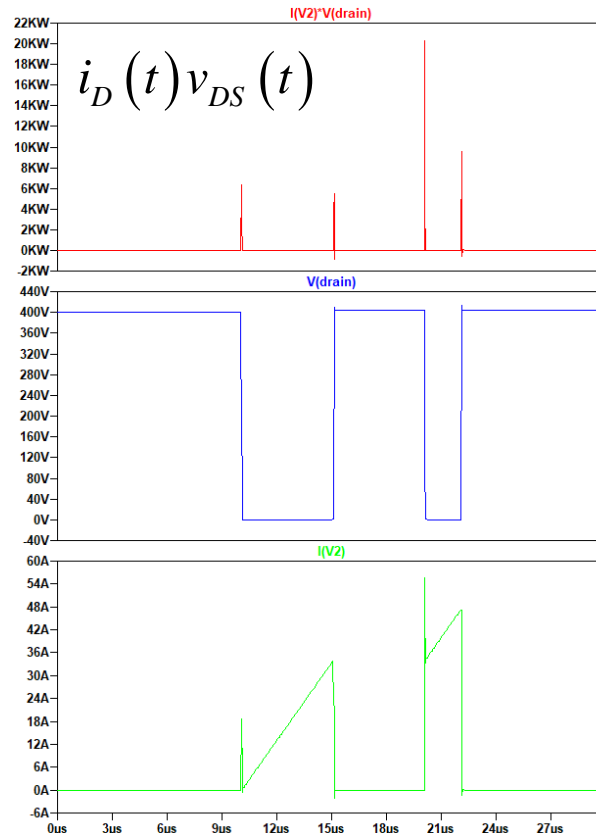
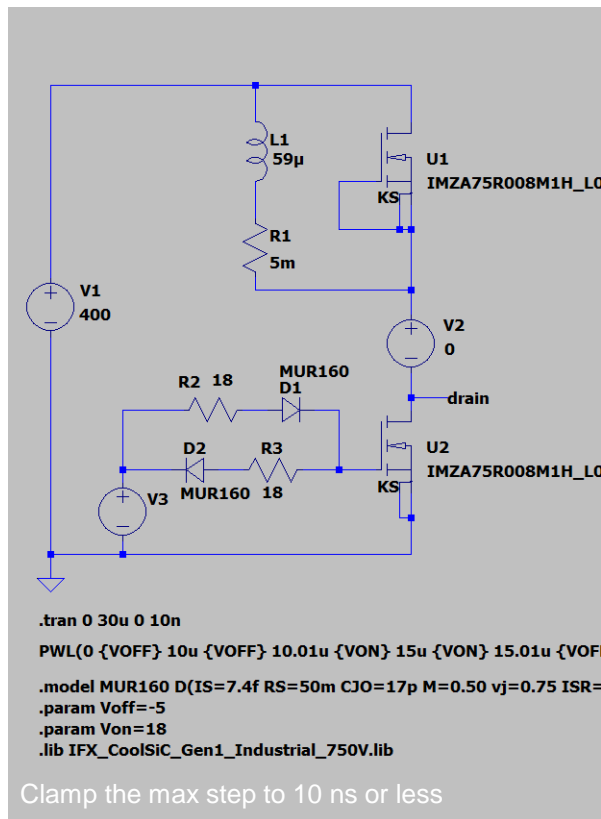


```
.SUBCKT SiCMOS_750V dd gg ss
*?@ Start SIMPLIS Encryption
.PARAM fpar1 = {8.148}
.PARAM fpar2 = {aabs/fpa}
.PARAM fpar3 = {abd_adj}
.PARAM fpar4 = {abdch_adj}
.PARAM fpar5 = {23.1}
.PARAM fpar6 = {aabs/fpa}
.PARAM fpar7 = {aabs_2*a}
.PARAM fpar8 = {rgint}
.PARAM fpar9 = {4.27}
.PARAM fpar10 = {17.67}
.PARAM fpar11 = {cgs_aa}
```



# Always check your SPICE Models!

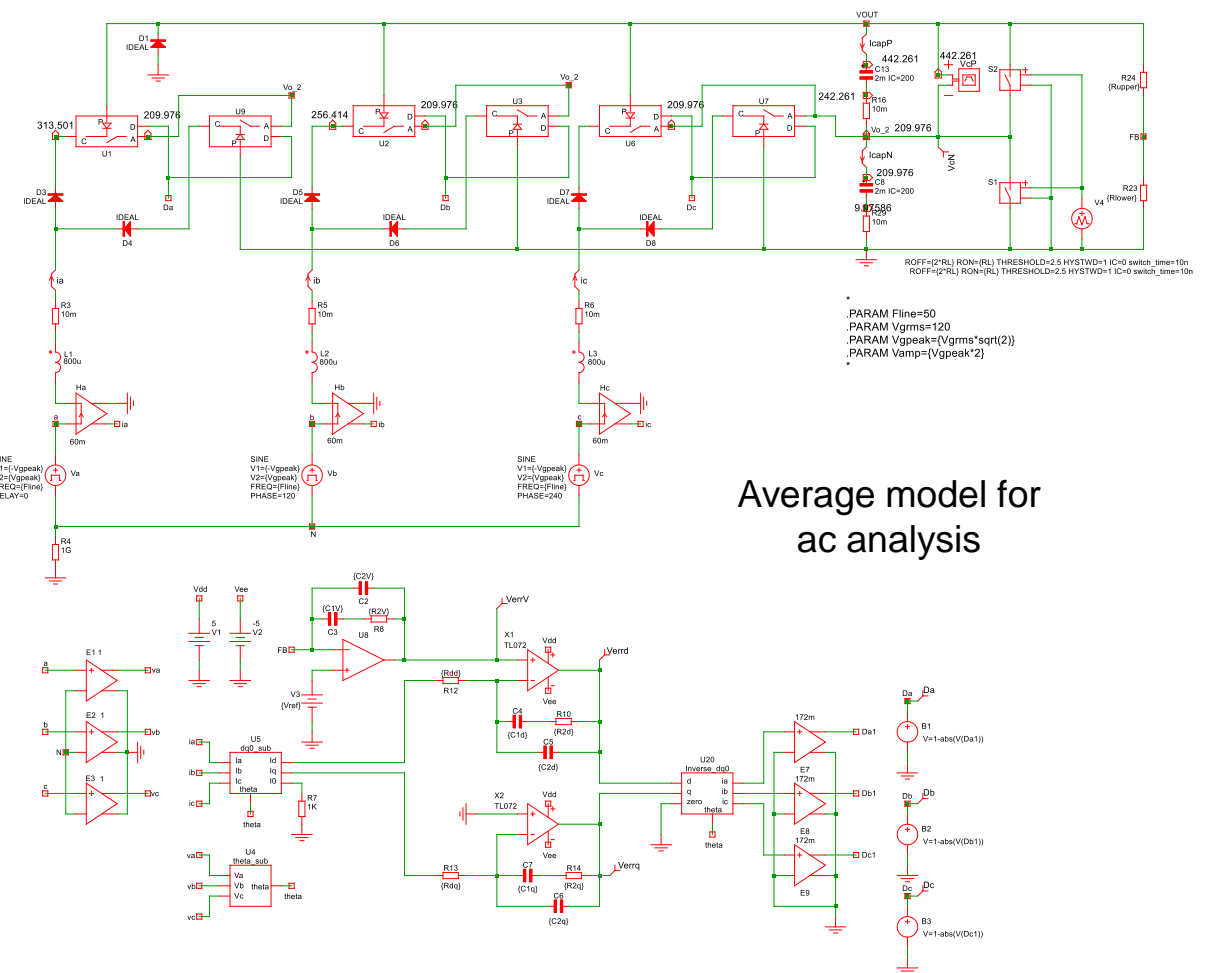
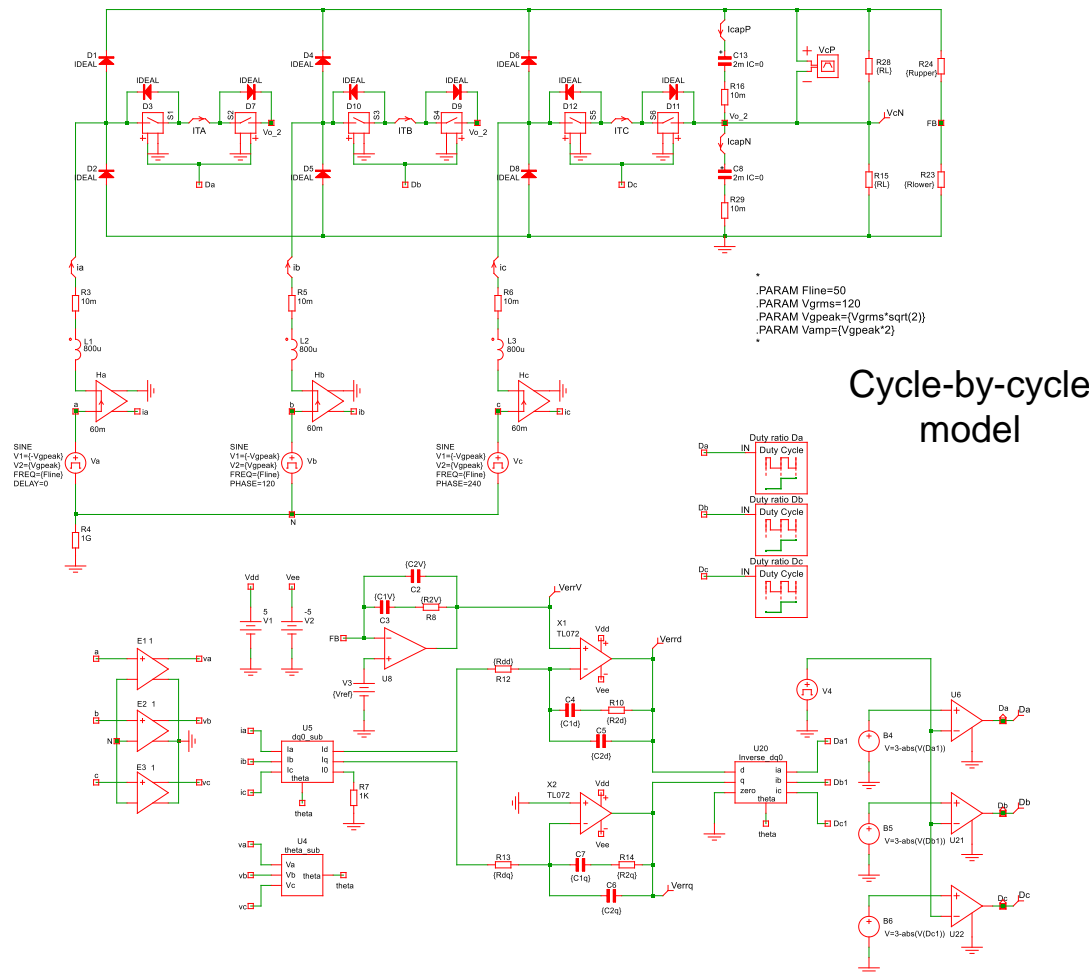
- An accurate model is necessary otherwise: garbage-in garbage out (GIGO)
- ✓ Implement a double-pulse test with the data-sheet conditions and check losses



PWL(0 {VOFF} 10u {VOFF} 10.01u {VON} 15u {VON} 15.01u {VOFF} 20u {VOFF} 20.01u {VON} 22u {VON} 22.01u {VOFF})

# Simulating a Vienna Rectifier

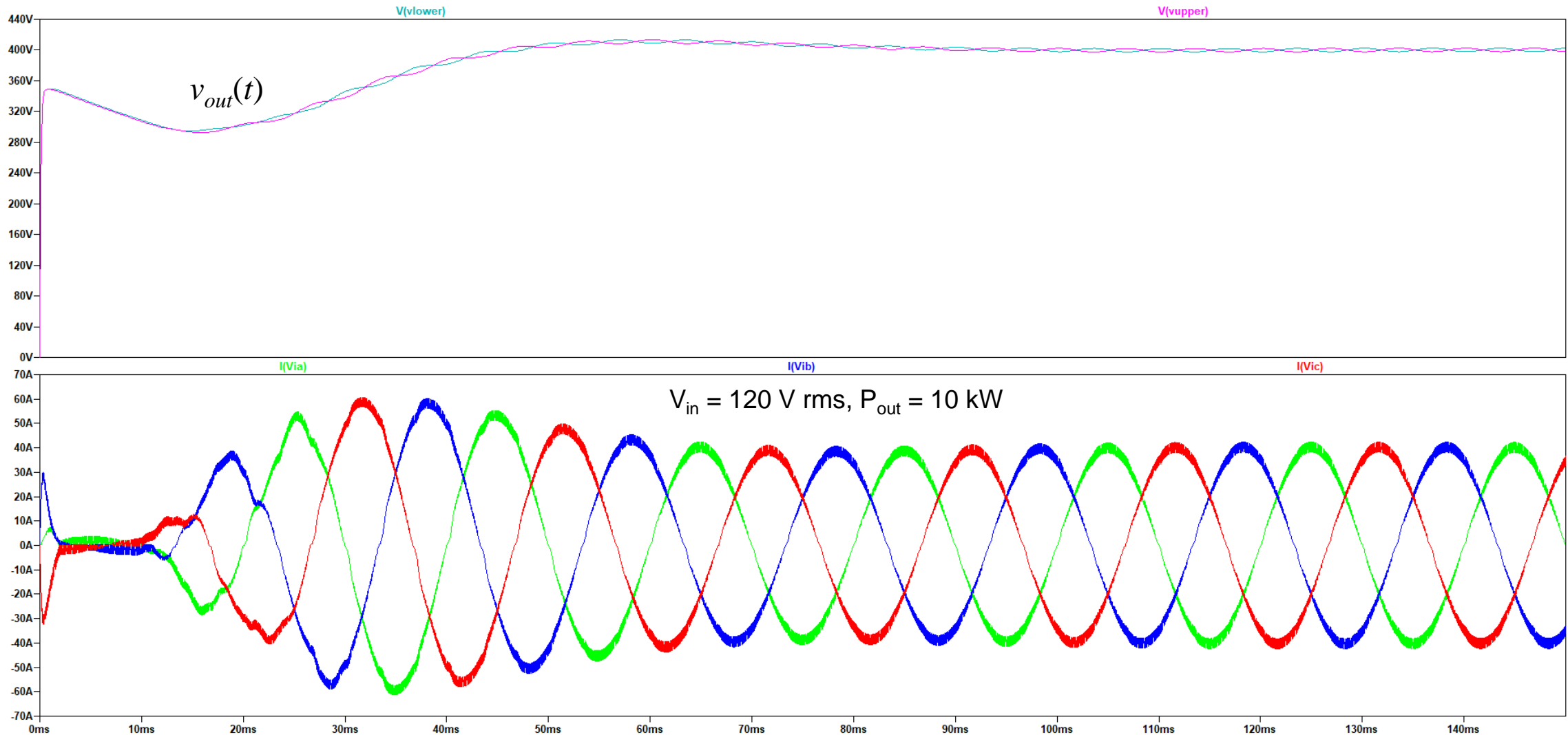
- The Vienna rectifier can be controlled using the dq0 blocks already available
- This 3-level converter requires two output capacitors, each biased at 400 V





# Simulation Results for a 10-kW Level

- The simulation is fast and the THD is 3.2% in this typical example



# Conclusion

- Power Factor correction is a hot topic for several decades
- In single-phase applications, analog implementation is still possible
- Different techniques are available with or without input voltage sensing
- The totem-pole PFC gains traction owing to modern semiconductors like GaN and SiC
- Three-phase PFC is a complex matter, and I recommend to study rotating machines first
- ✓ Many terms and mathematical expressions come from this field
- Most of the 3-phase PFC projects I have seen deal with digital control
- Simulation helps a lot for assessing losses but also for conveniently closing the loop

I'm done, merci, thank you  
und danke vielmals!

I don't care about PFCs when I cycle in the mountains!

