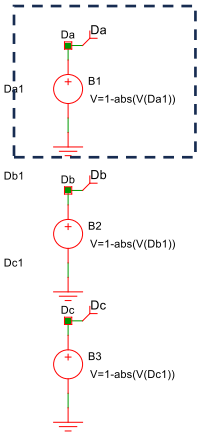
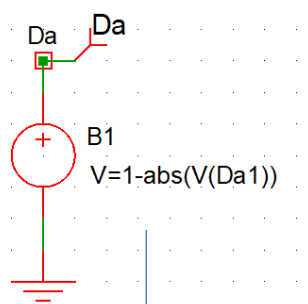
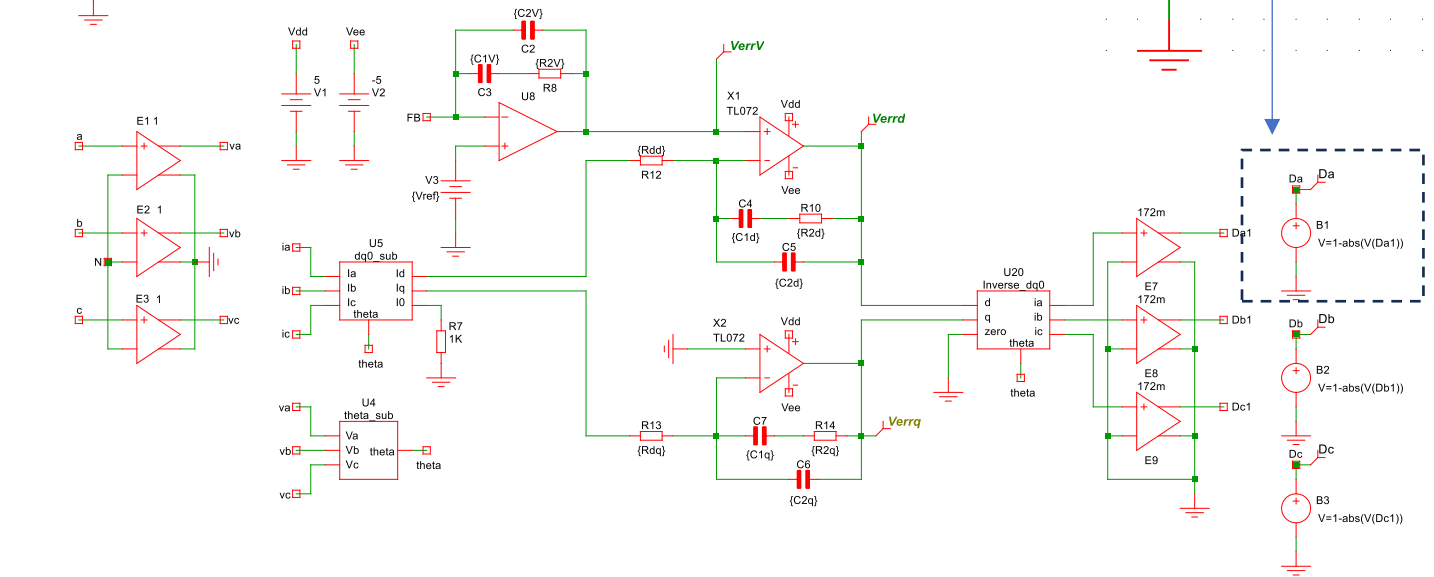


```

.PARAM Fline=50
.PARAM Vgrms=120
.PARAM Vgpeak={Vgrms*sqrt(2)}
.PARAM Vamp={Vgpeak*2}

```

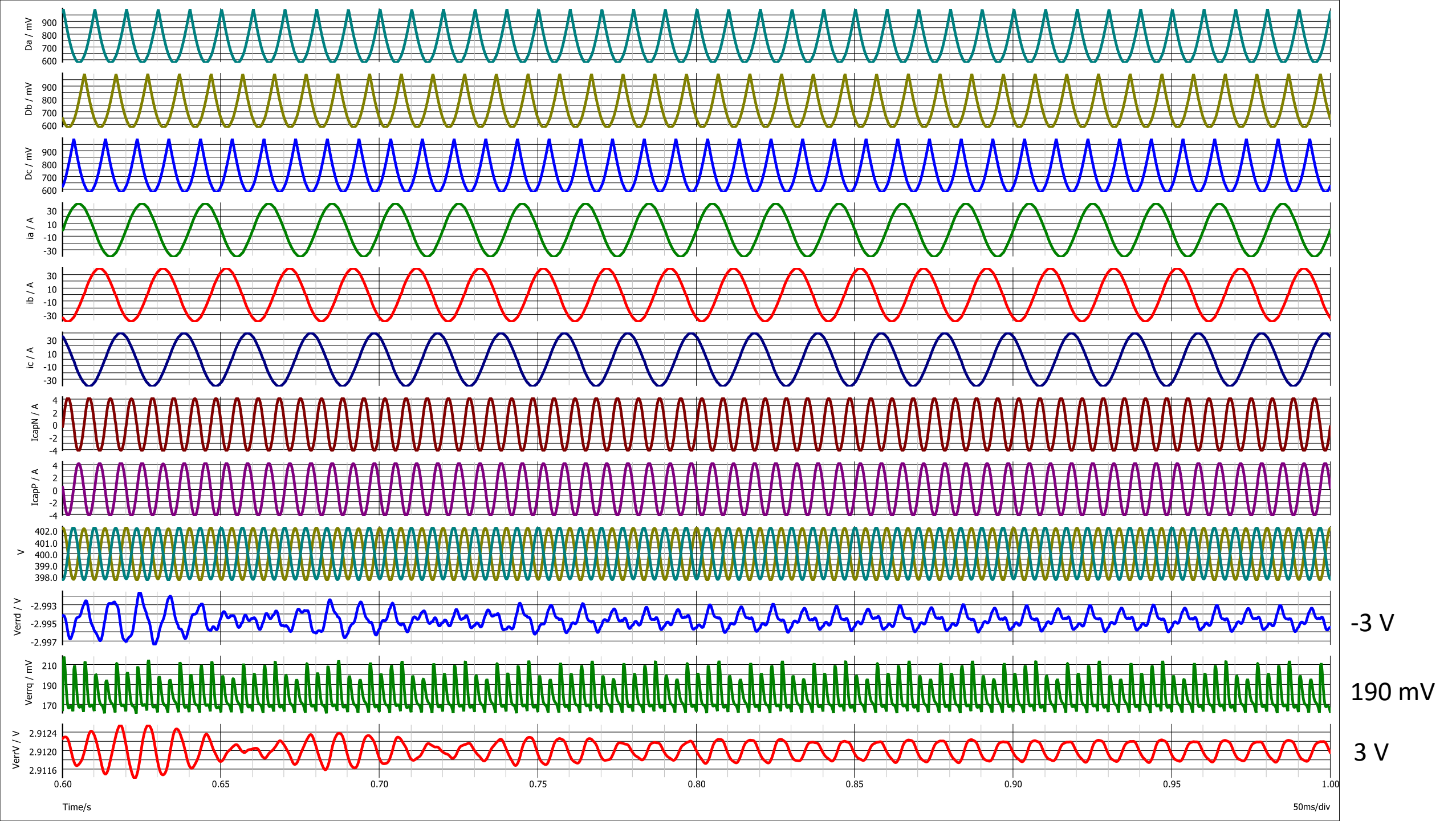


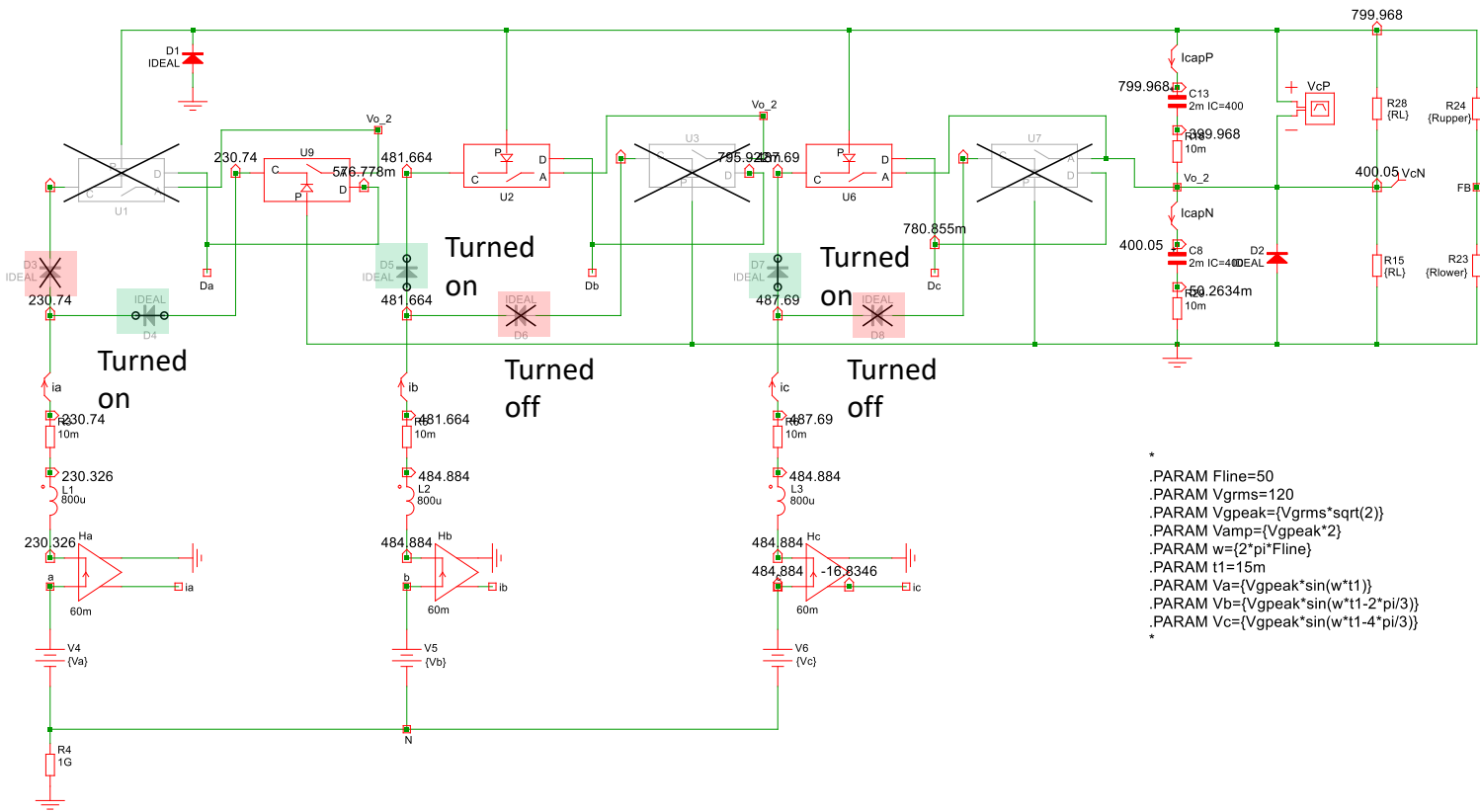
This is an averaged version of the Vienna rectifier using the model of the PWM switch. The PFC delivers 800 V for a 10-kW load. This is a low-line simulation ( $V_{in} = 120$  V rms) to check the control section.

The dq0 modulator-demodulator is similar to the one used in the 6-pack example. An additional treatment is added in the output of the modulator to produce an off-time modulation (1-D) for this Vienna application.

This averaged model is used later to extract the ac response of the three loops and stabilize the converter.

I have appreciated interacting with Yang Fu from Shenzhen - 多谢!





```

.PARAM Fline=50
.PARAM Vgrms=120
.PARAM Vgpeak={Vgrms*sqrt(2)}
.PARAM Vamp={Vgpeak*2}
.PARAM w={2*pi*Fline}
.PARAM t1=15m
.PARAM Va={Vgpeak*sin(w*t1)}
.PARAM Vb={Vgpeak*sin(w*t1-2*pi/3)}
.PARAM Vc={Vgpeak*sin(w*t1-4*pi/3)}

```

For the dc operating point, I believe only some averaged models need to be active at a time considering the input line polarities at the selected time  $t_1$ . Here, I selected 15 ms implying:

$$t_{10} = 15\text{ms}$$


---

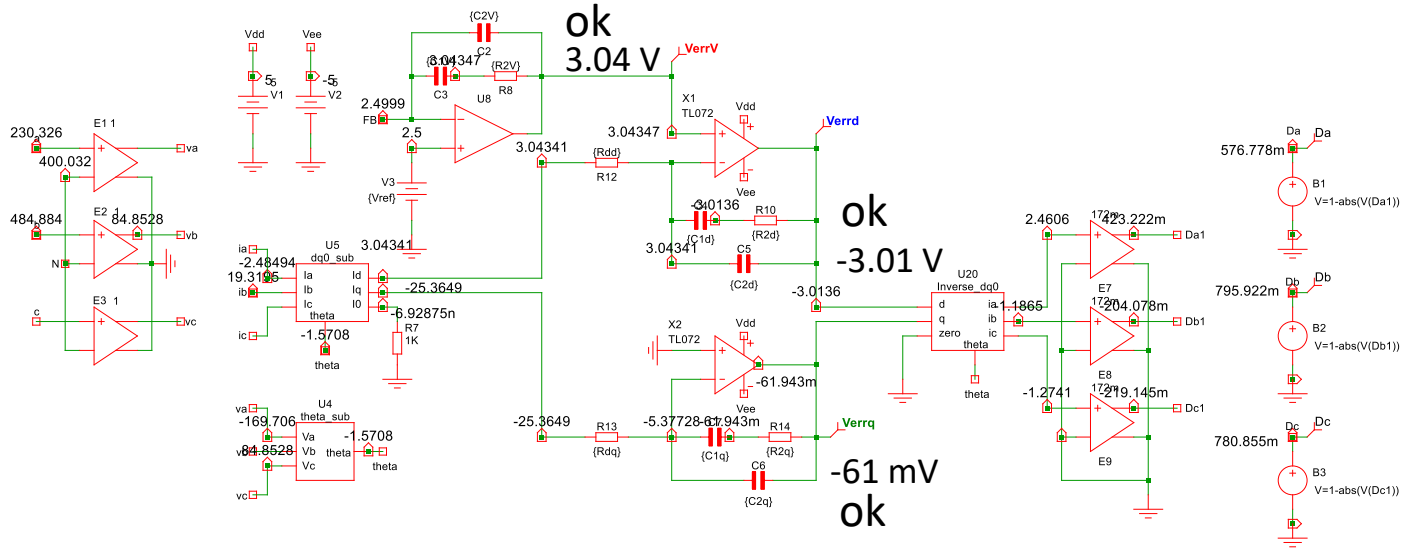

$$v_a(t_{10}) = -169.706\text{ V} \quad \text{neg}$$

$$v_b(t_{10}) = 84.853\text{ V} \quad \text{pos}$$

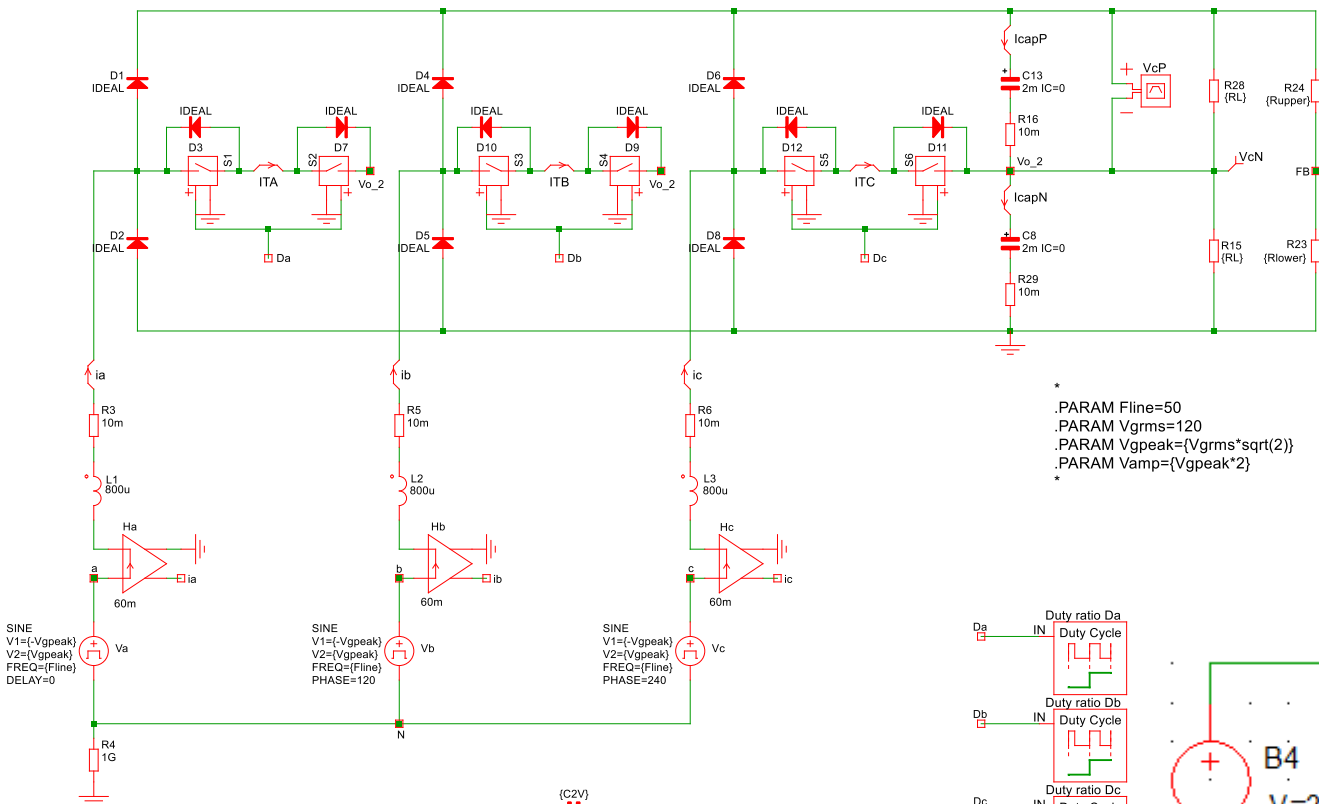
$$v_c(t_{10}) = 84.853\text{ V} \quad \text{pos}$$

$$\theta = \text{atan2}(v_{\cos}(t_{10}), v_{\sin}(t_{10})) = -1.571$$

This selection implies that positive diodes on line b and c are turned on. The diode on the negative line a is active. Some of the models are turned off, easing the burden on the simulation engine.



The operating point seems correct and matches the transient simulation. Using three averaged models (or 6 in the transient simulation), makes the simulation sensitive to any parameter change: always check the dc point is ok.



```

.PARAM Fline=50
.PARAM Vgrms=120
.PARAM Vgpeak={Vgrms*sqrt(2)}
.PARAM Vamp={Vgpeak*2}

```

```

SINE
V1={-Vgpeak}
V2={Vgpeak}
FREQ={Fline}
DELAY=0

```

```

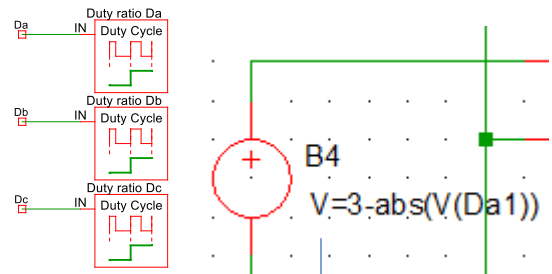
SINE
V1={-Vgpeak}
V2={Vgpeak}
FREQ={Fline}
PHASE=120

```

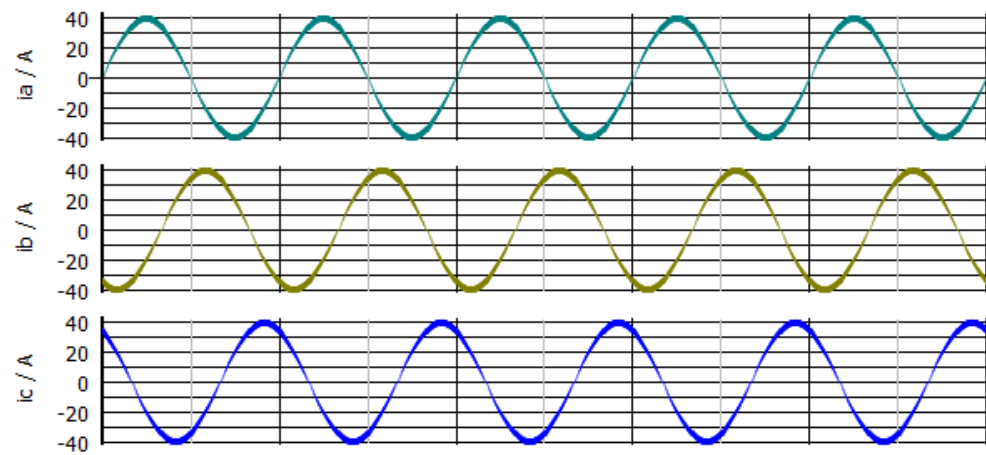
```

SINE
V1={-Vgpeak}
V2={Vgpeak}
FREQ={Fline}
PHASE=240

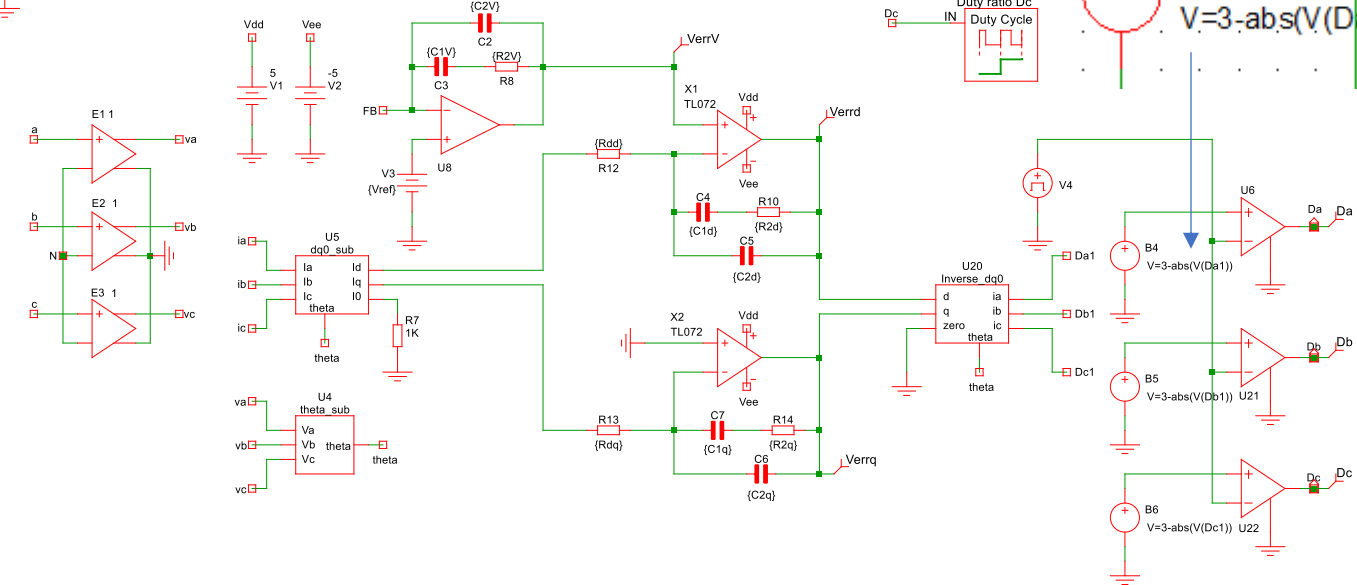
```

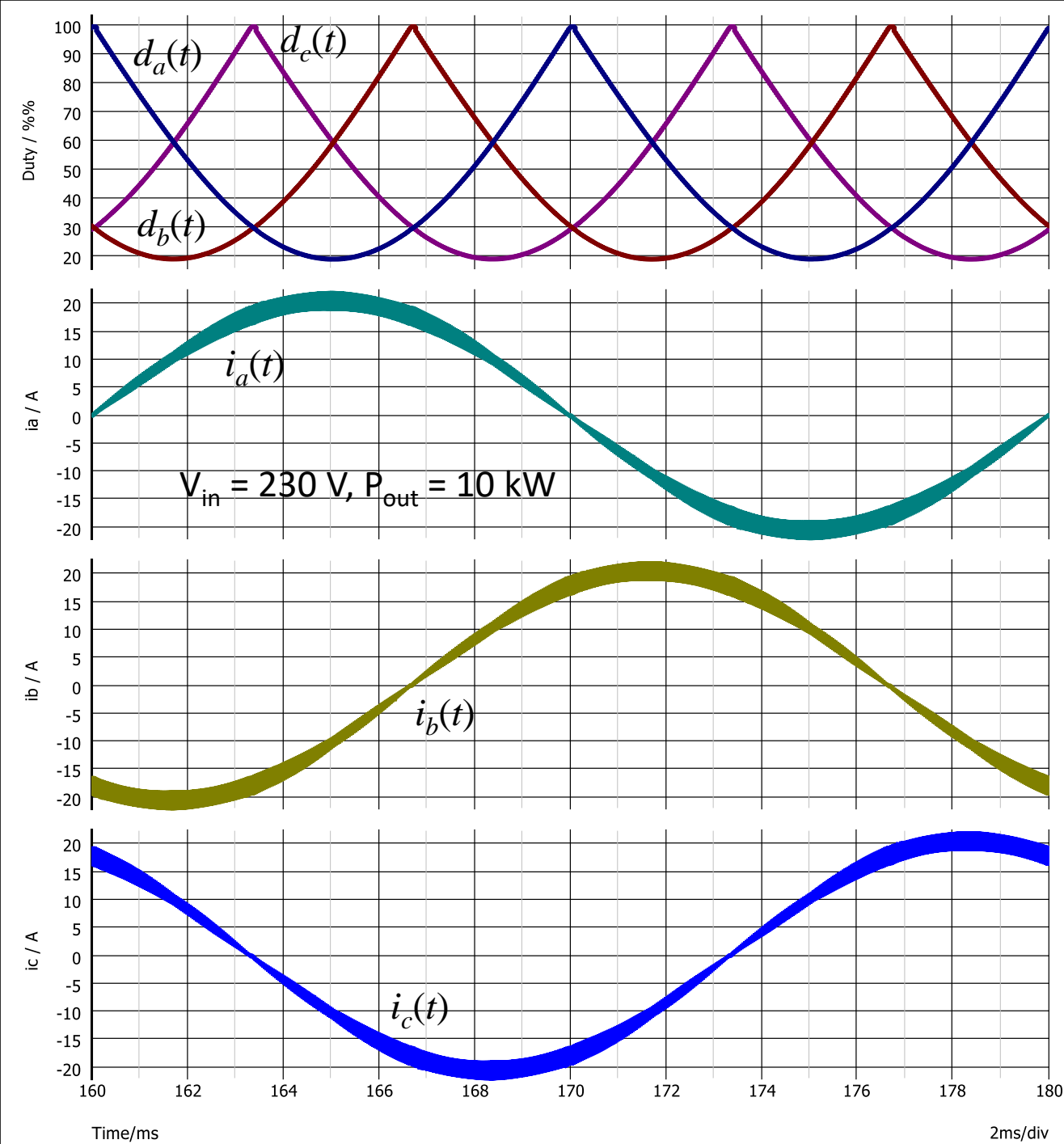


This is the cycle-by-cycle simulation. The output voltage is 800 V,  $P_{out} = 10 \text{ kW}$

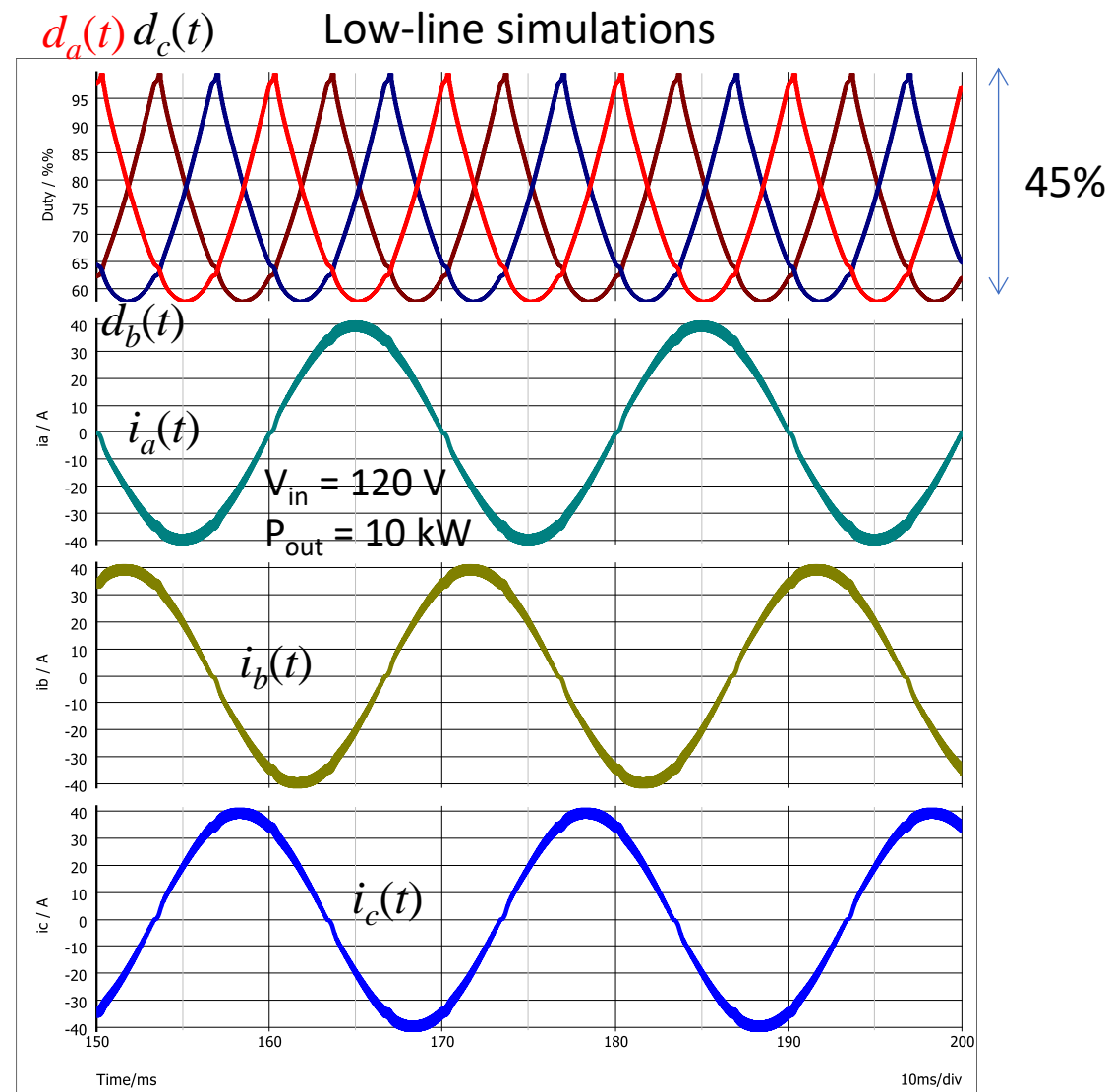


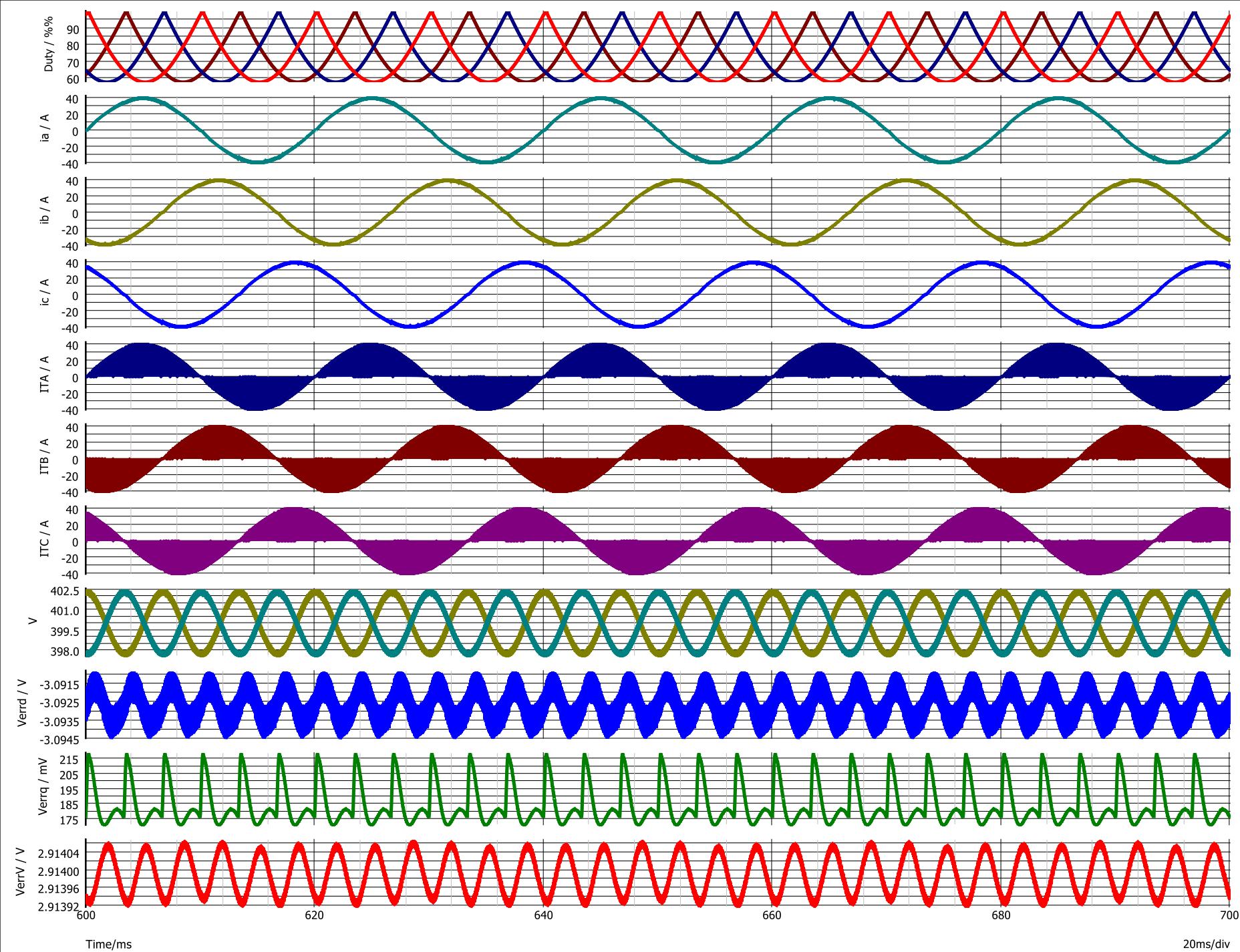
ia Distortion/cycle 3.64304%  
 ib Distortion/cycle 3.19371%  
 ic Distortion/cycle 3.62285%





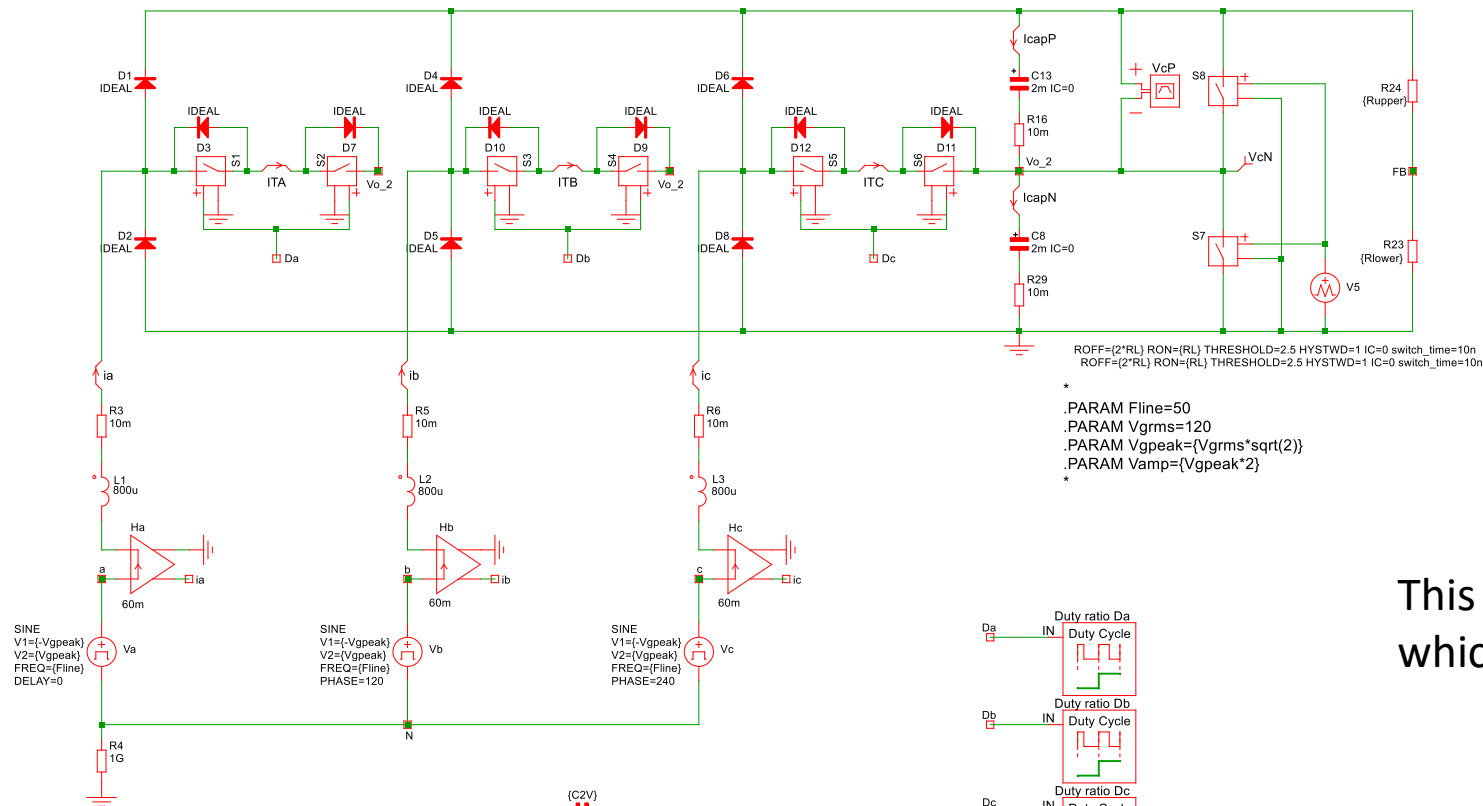
This is the way the duty ratio is elaborated to force sinusoidal input currents to the Vienna converter. The modulation depth is adjusted depending on operating conditions.





The cycle-by-cycle simulation confirms the operating points are good. The voltage is well spread between the two output capacitors for an 800-V rail. The values for the  $d$ ,  $q$  and error voltage do match the averaged simulations.





```

ROFF=(2*RL) RON={RL} THRESHOLD=2.5 HYSTWD=1 IC=0 switch_time=10n
ROFF=(2*RL) RON={RL} THRESHOLD=2.5 HYSTWD=1 IC=0 switch_time=10n
.PARAM Fline=50
.PARAM Vgrms=120
.PARAM Vgpeak={Vgrms*sqrt(2)}
.PARAM Vamp={Vgpeak*2}

```

```

SINE
V1={-Vgpeak}
V2={Vgpeak}
FREQ={Fline}
DELAY=0

```

```

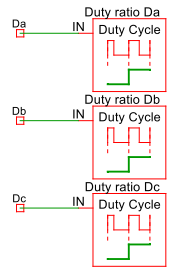
SINE
V1={-Vgpeak}
V2={Vgpeak}
FREQ={Fline}
PHASE=120

```

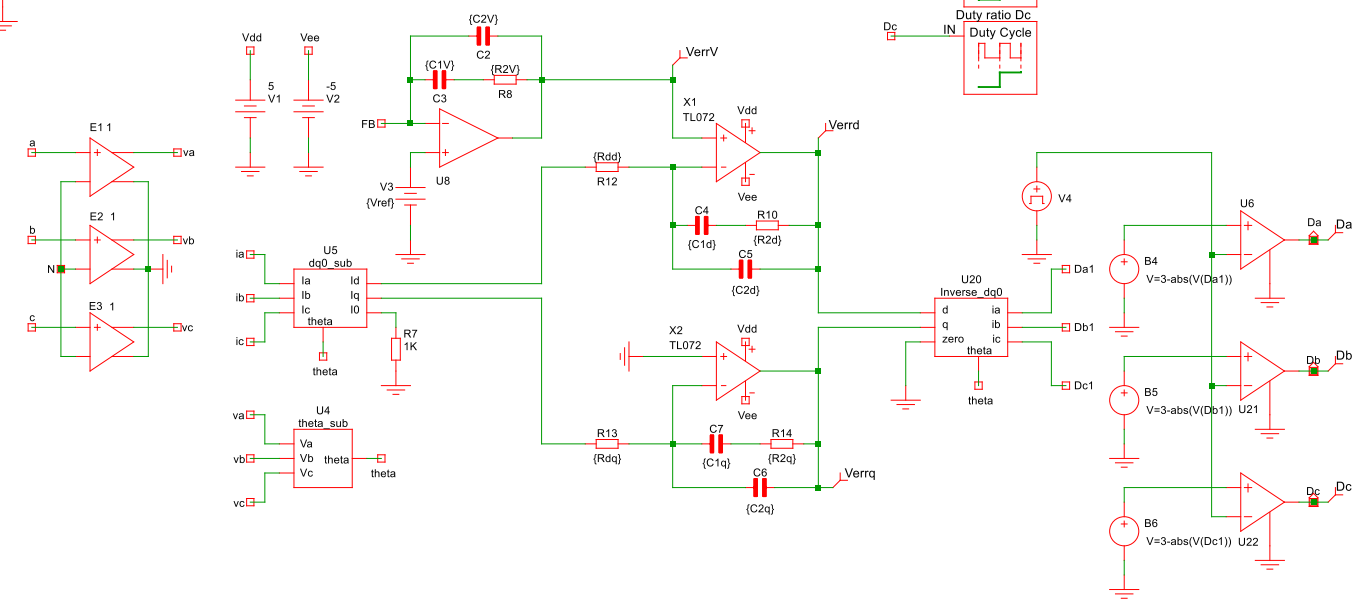
```

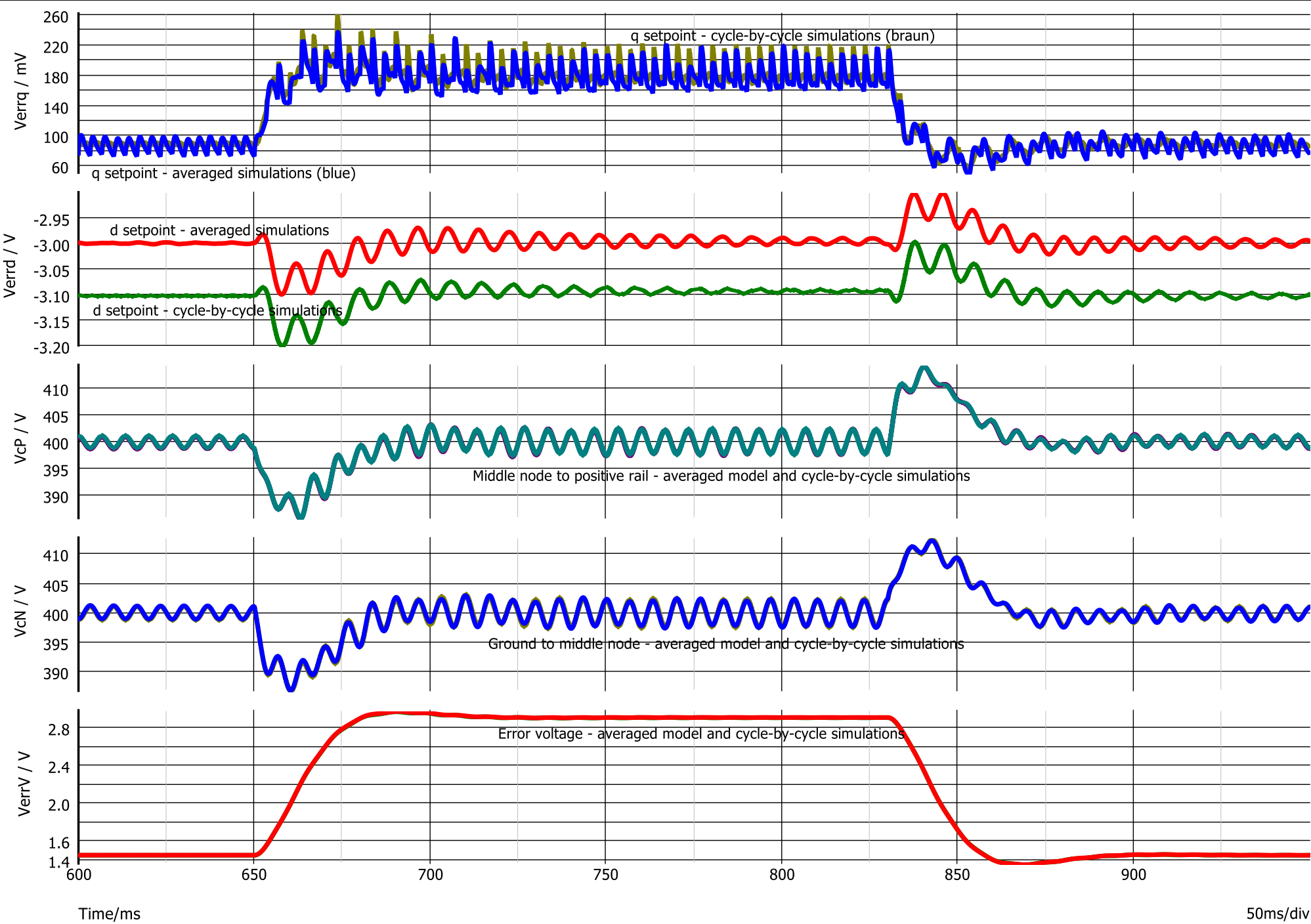
SINE
V1={-Vgpeak}
V2={Vgpeak}
FREQ={Fline}
PHASE=240

```



This is a transient cycle-by-cycle simulation in which the load is stepped from  $P_{out}/2$  to  $P_{out}$ .

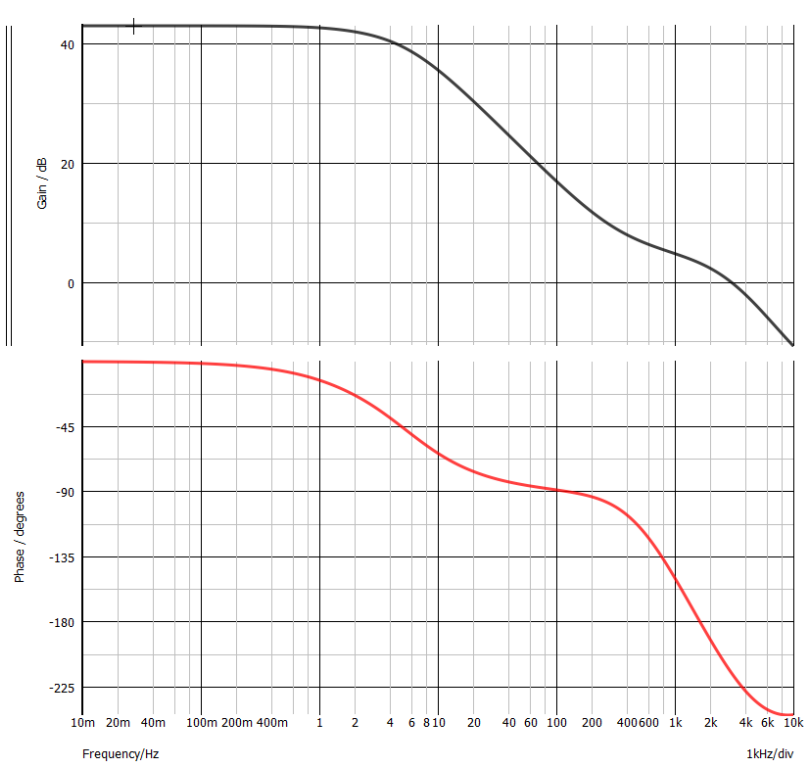




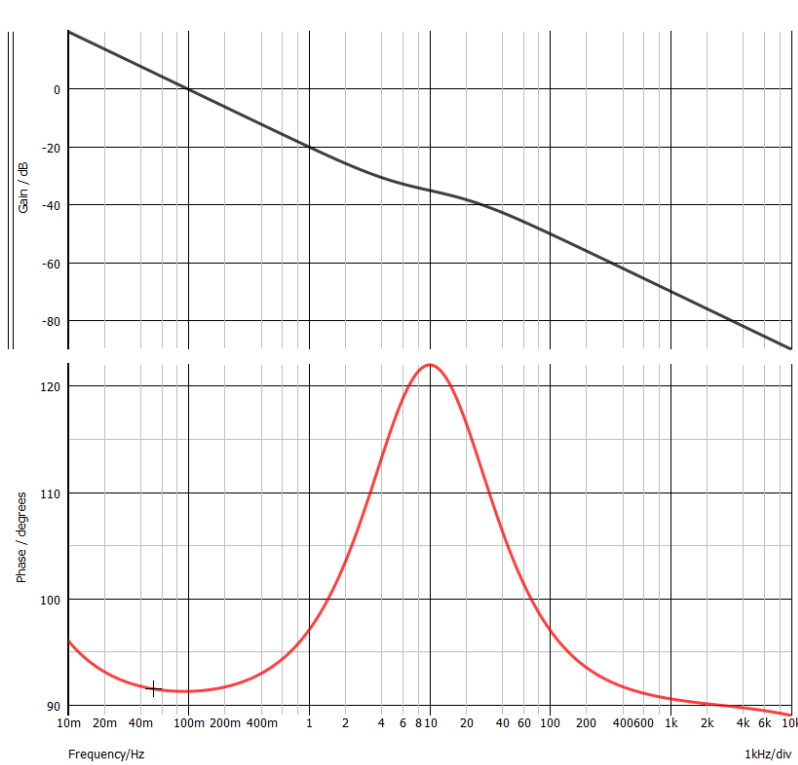
Excellent match between averaged and cycle-by-cycle simulations. There is a slight offset on the d levels but nothing serious.

Having averaged and cycle-by-cycle data well superimposed is a great reward and confirms the modeling approach.

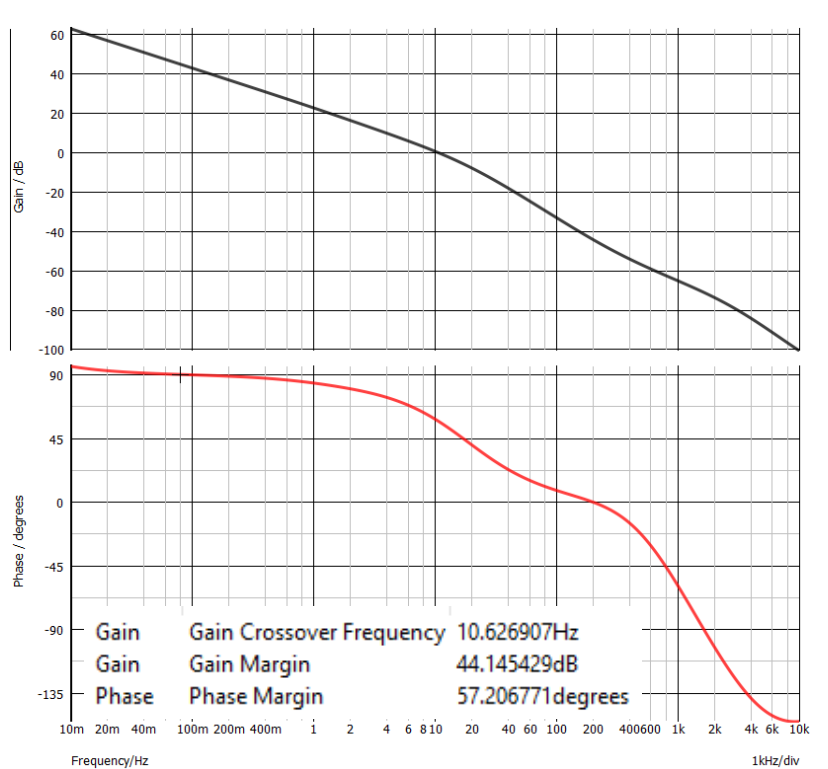




Power stage

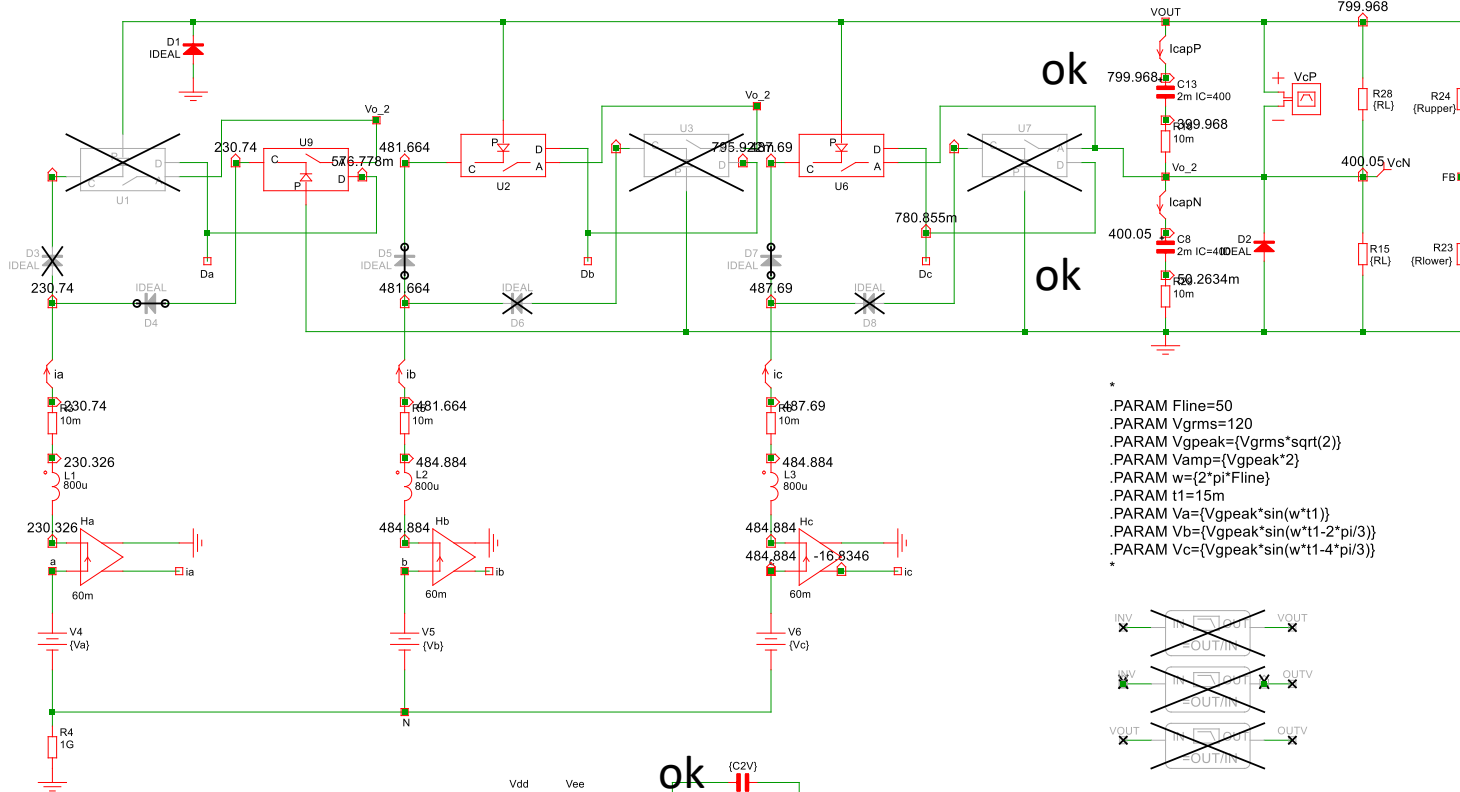


Type 2 centered at 10 Hz



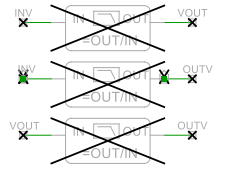
Compensated V loop

In the previous slide, you can see that some of the PWM switch models are grayed out. The reason is that I have selected a  $t_1$  value (15 ms) for which  $V_a$  is negative (-169 V) while  $V_b$  and  $V_c$  are positive at 84 V. As such, the PWM switch model in  $V_a$  treating the positive polarity is made silent (grayed out) while only the one dealing with the negative value is active. Same with the models undergoing the negative polarities for  $V_b$  and  $V_c$ , they are also grayed out and only the ones treating the positive waves are active. The grayed-out models would normally be ignored by the engine considering the series diodes but the lighter the circuitry is, the easier it becomes for converging and finding a correct bias point.

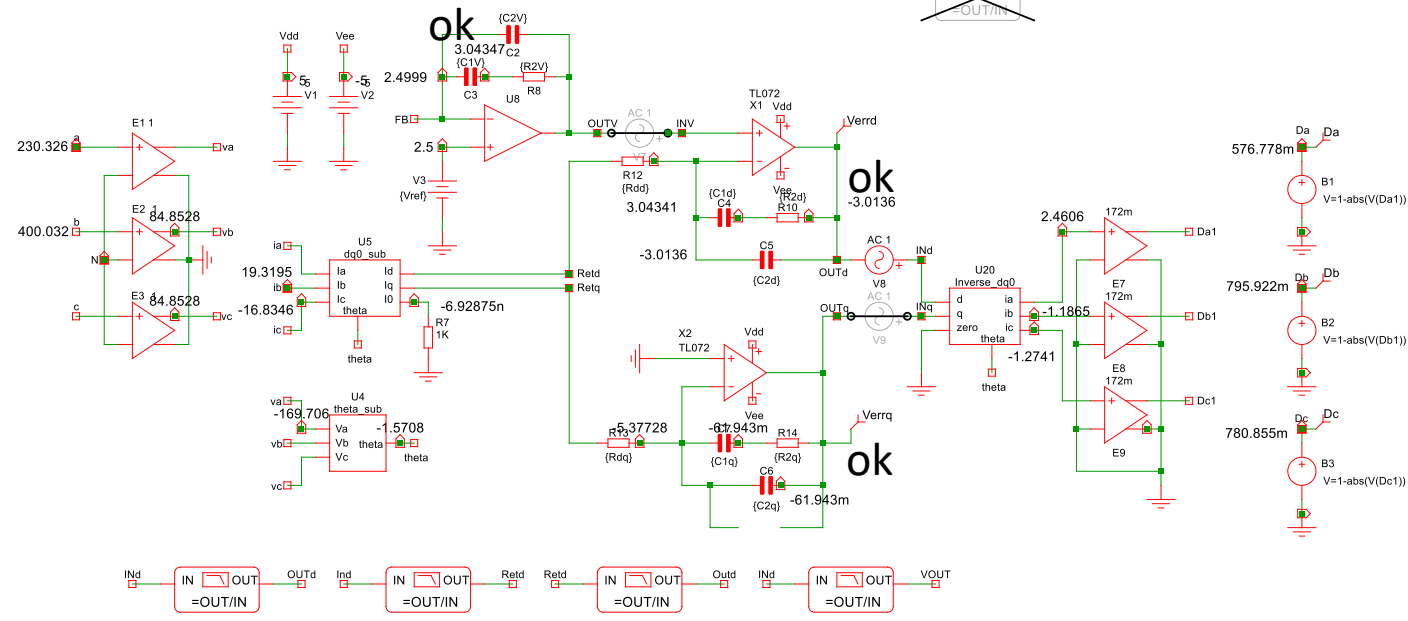


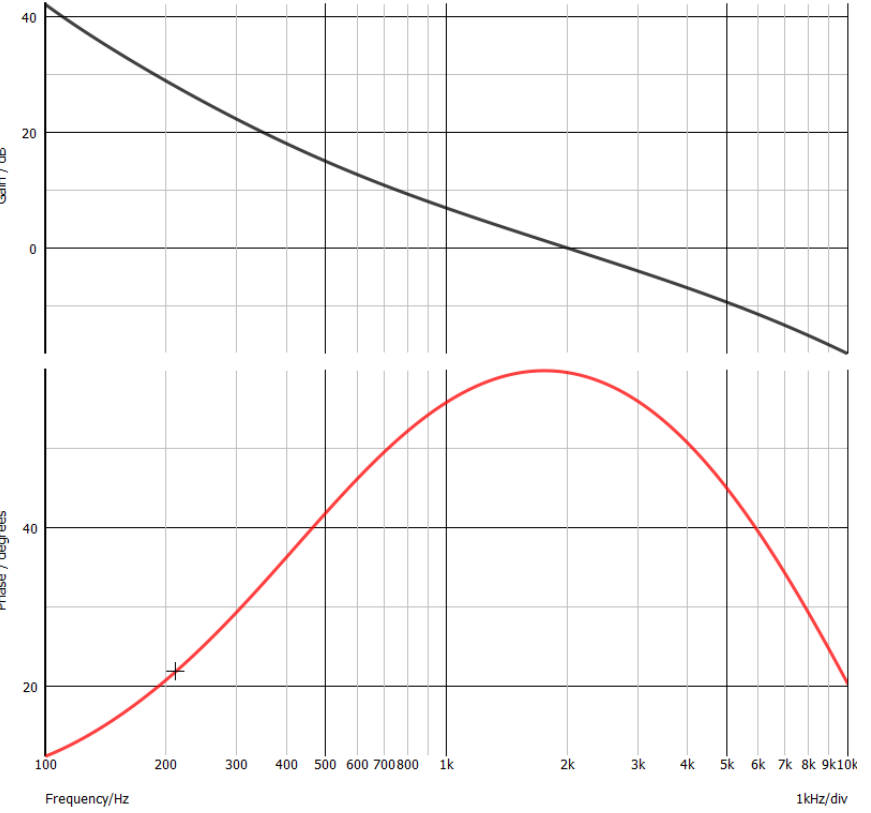
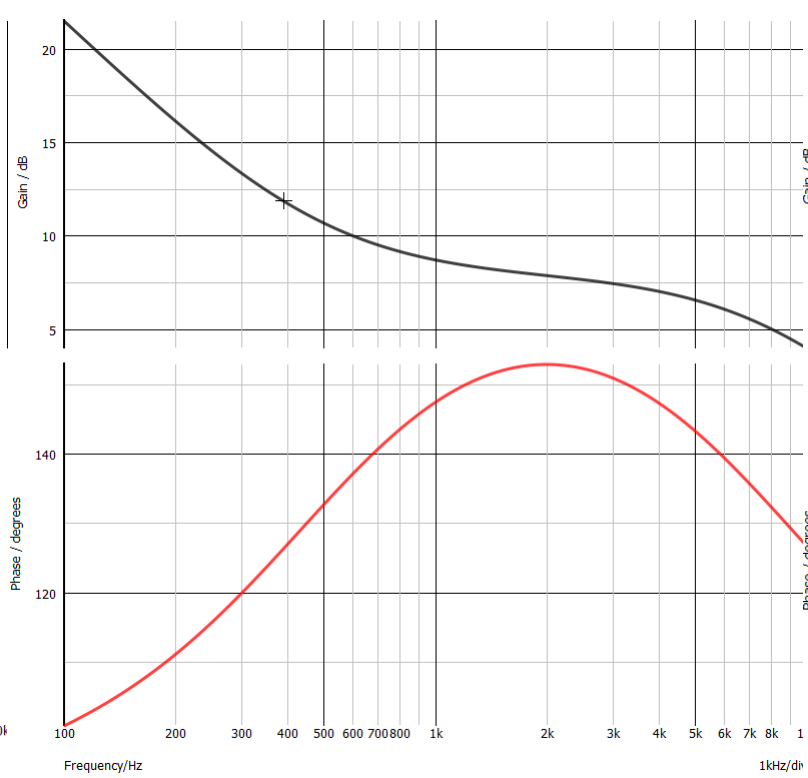
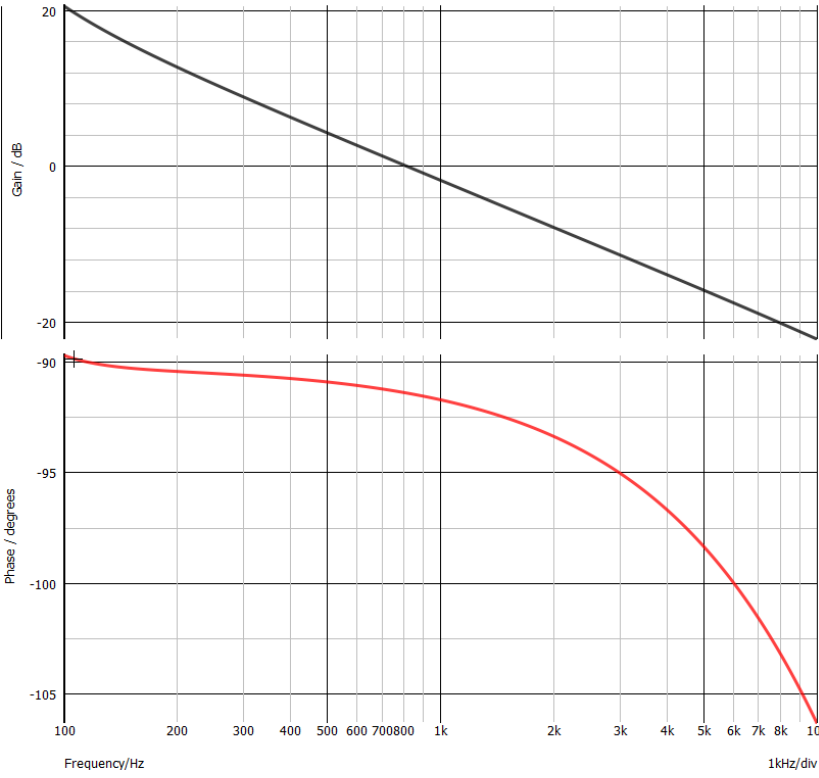
```

.PARAM Fline=50
.PARAM Vgrms=120
.PARAM Vgpeak=(Vgrms*sqrt(2))
.PARAM Vamp=(Vgpeak*2)
.PARAM w={2*pi*Fline}
.PARAM t1=15m
.PARAM Va={Vgpeak*sin(w*t1)}
.PARAM Vb={Vgpeak*sin(w*t1-2*pi/3)}
.PARAM Vc={Vgpeak*sin(w*t1-4*pi/3)}
  
```



Now validate the d loop measurement. Check operating point are ok still.



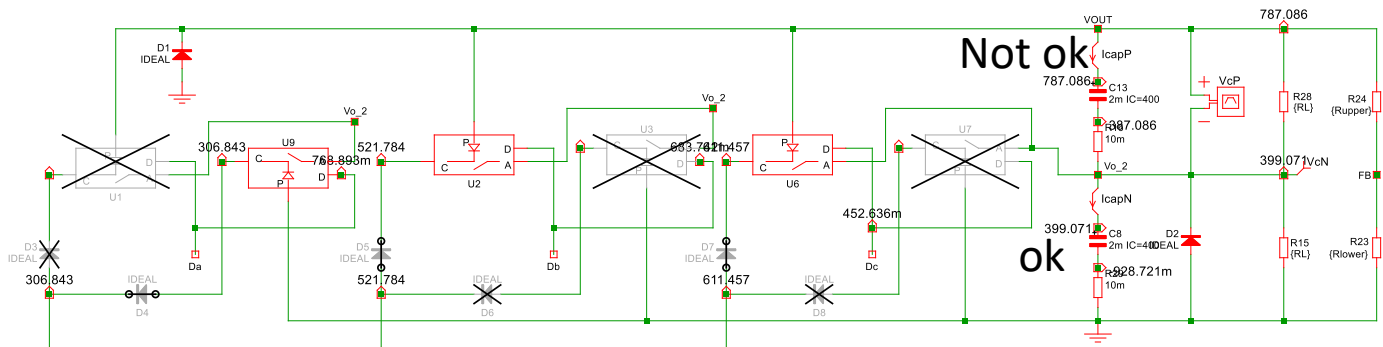


Power stage of d loop

Type 2 centered at 2 kHz

Gain	Gain Crossover Frequency	2.0142727kHz
Gain	Gain Margin	***ERROR***
Phase	Phase Margin	59.511622degrees

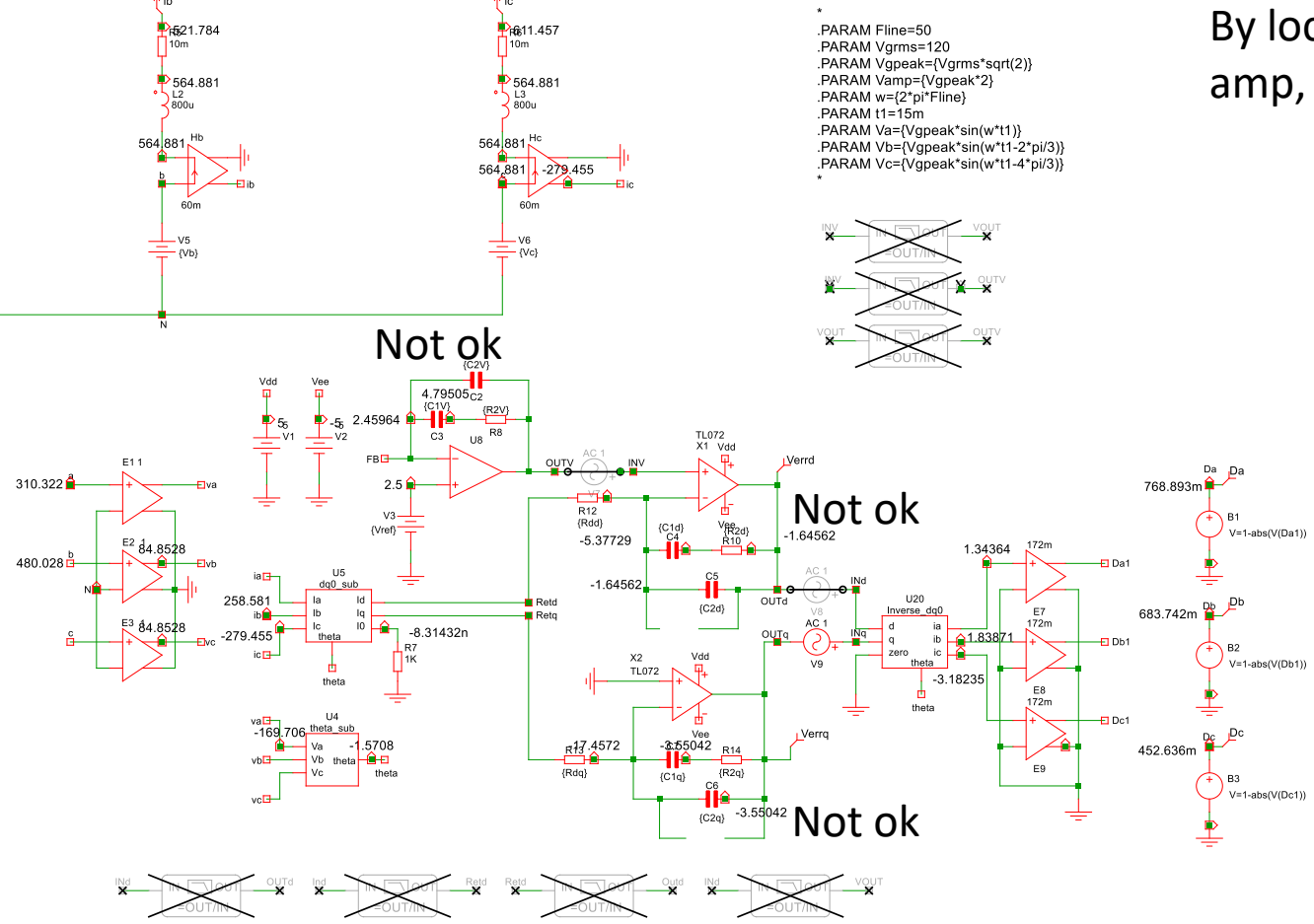
Compensated d loop



Not ok  
ok

Now enable the q loop. In theory, both d and q loops have the same transfer function but it is always interesting to look at each individually. Here, by enabling the ac source with the q loop, the operating point is wrong.

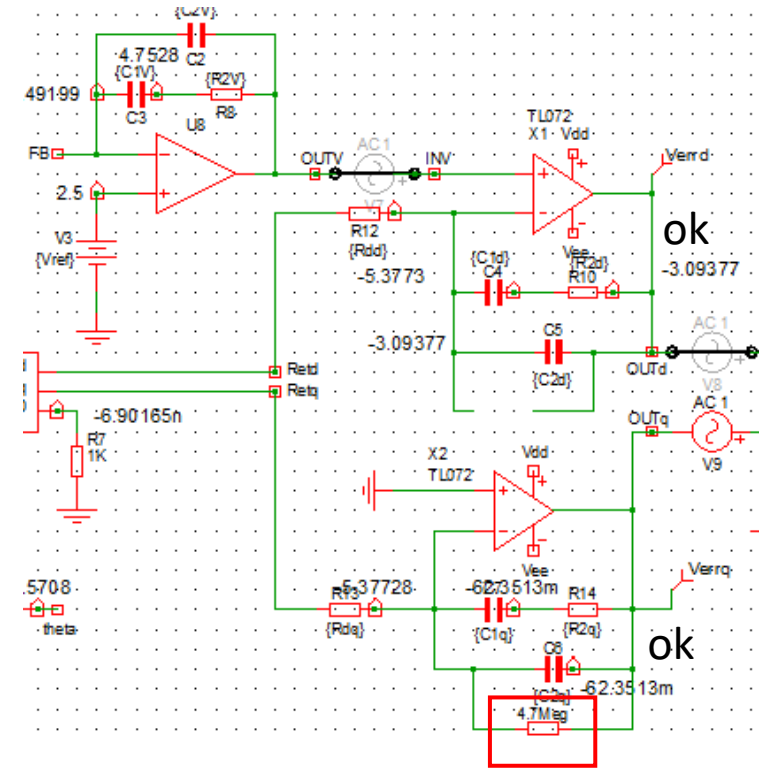
By locally reducing the open-loop gain of the q op-amp, the circuit converges:



Not ok

Not ok

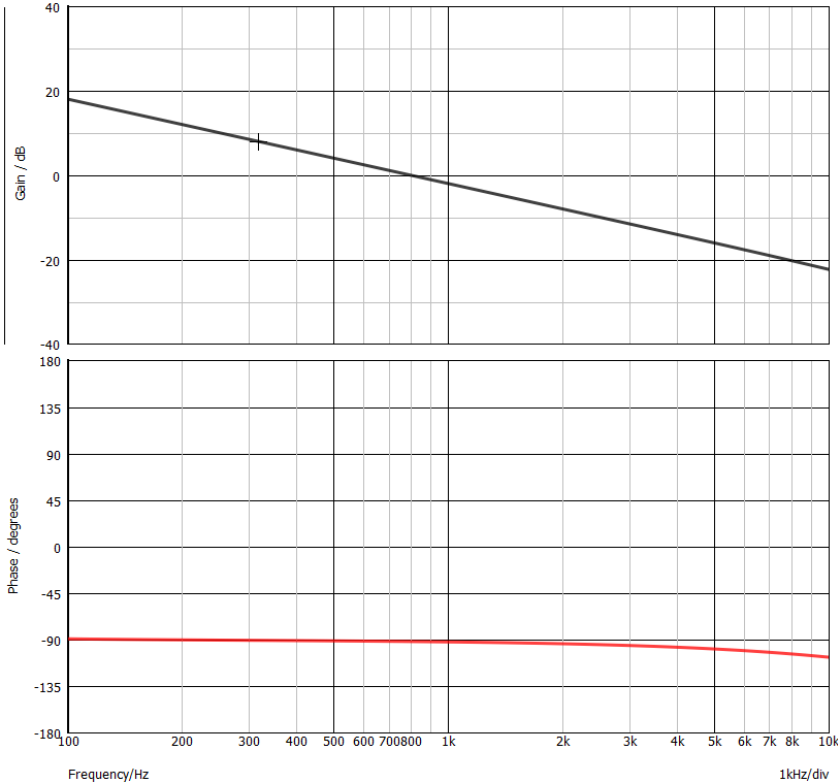
Not ok



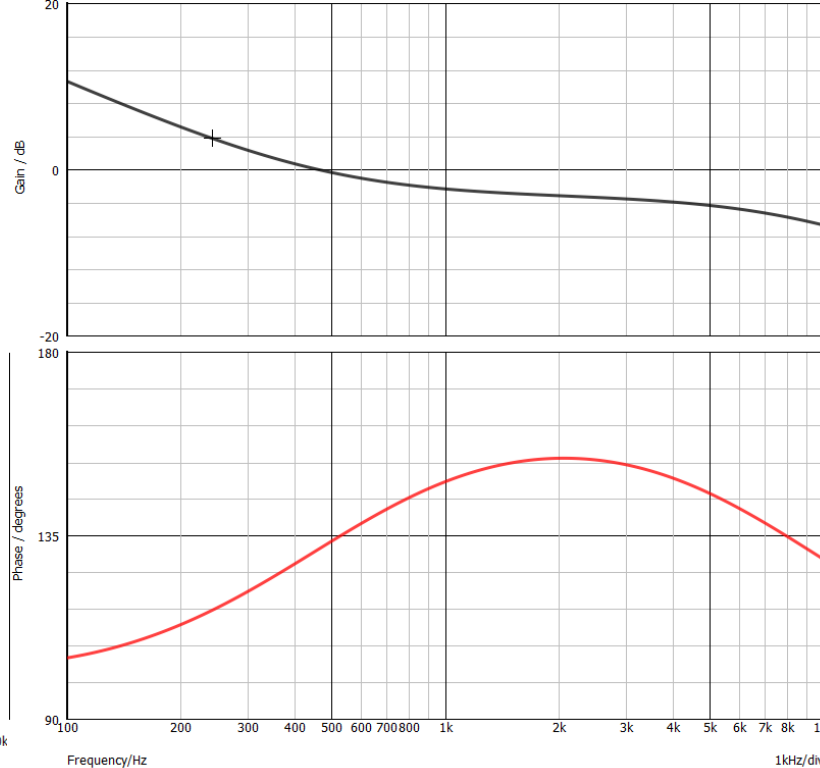
ok

ok

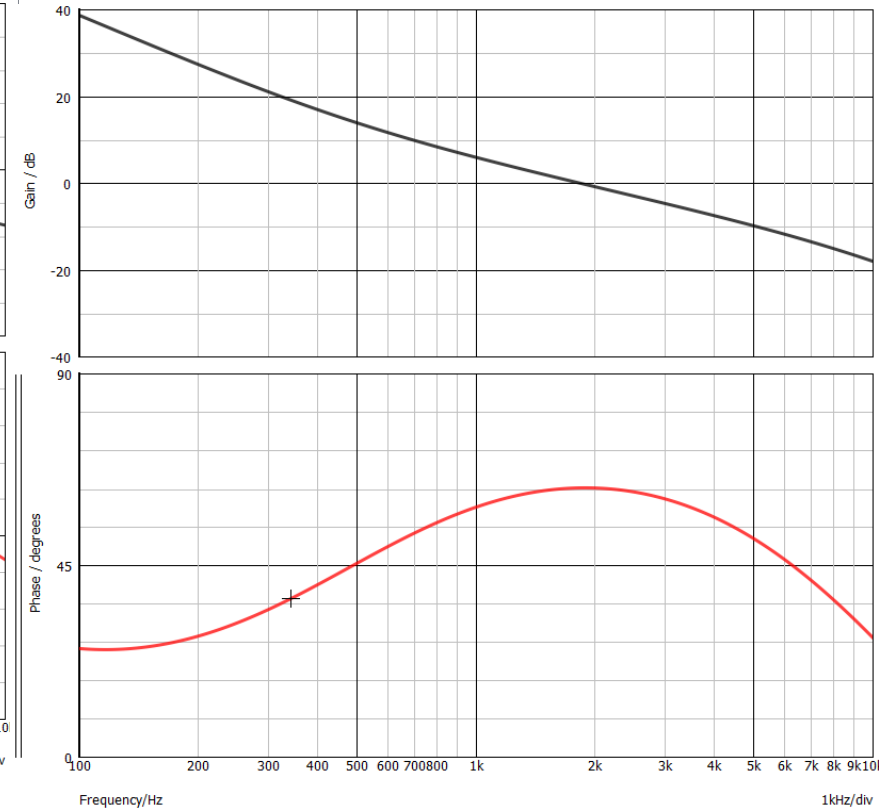
Added resistance  
Remove it for other analyses



Power stage of q loop

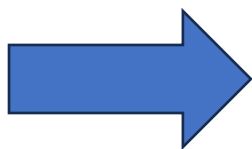


Type 2 centered at 2 kHz



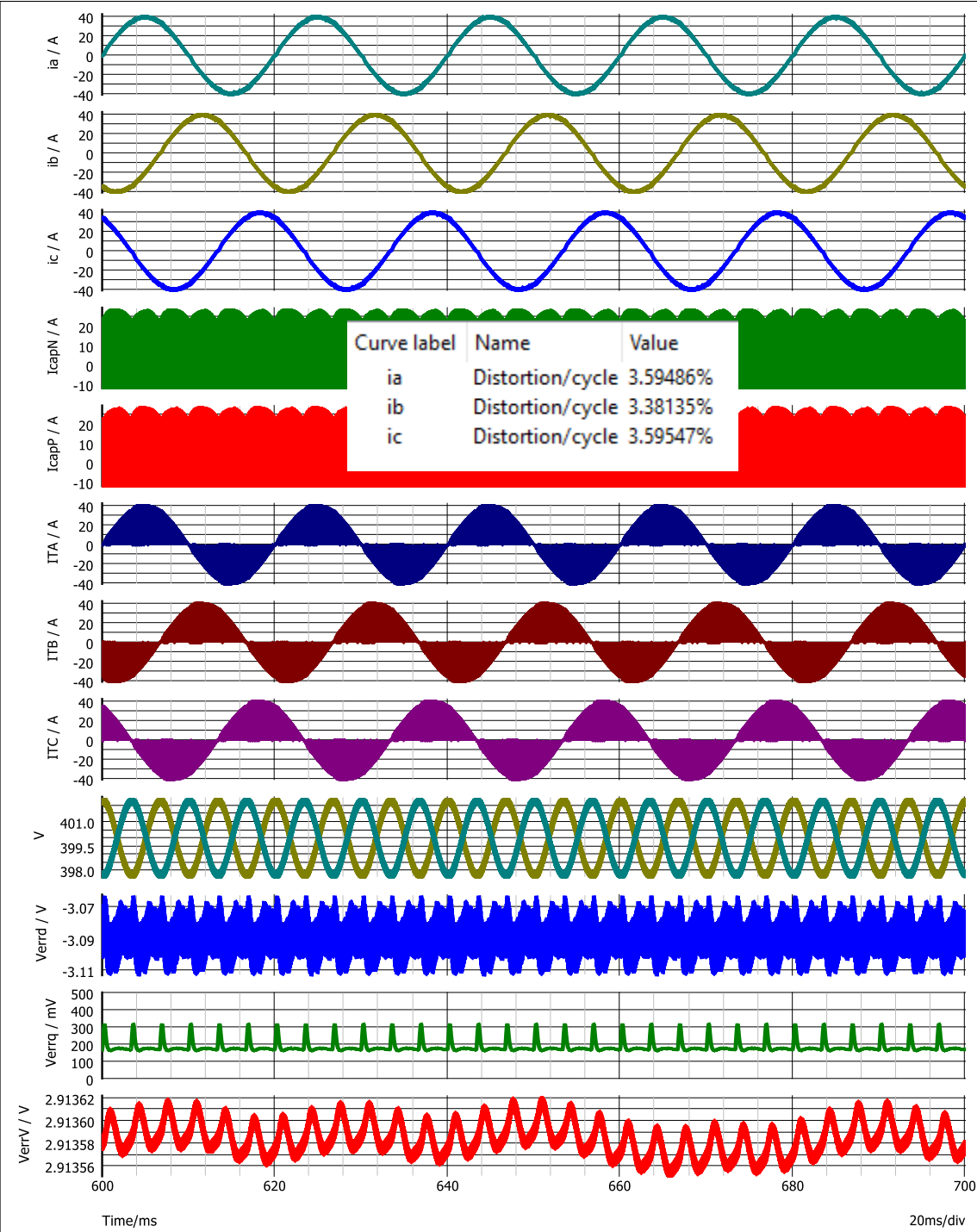
Compensated d loop

Finally, I have set the voltage loop at 10 Hz and the dq loops at 1 kHz.



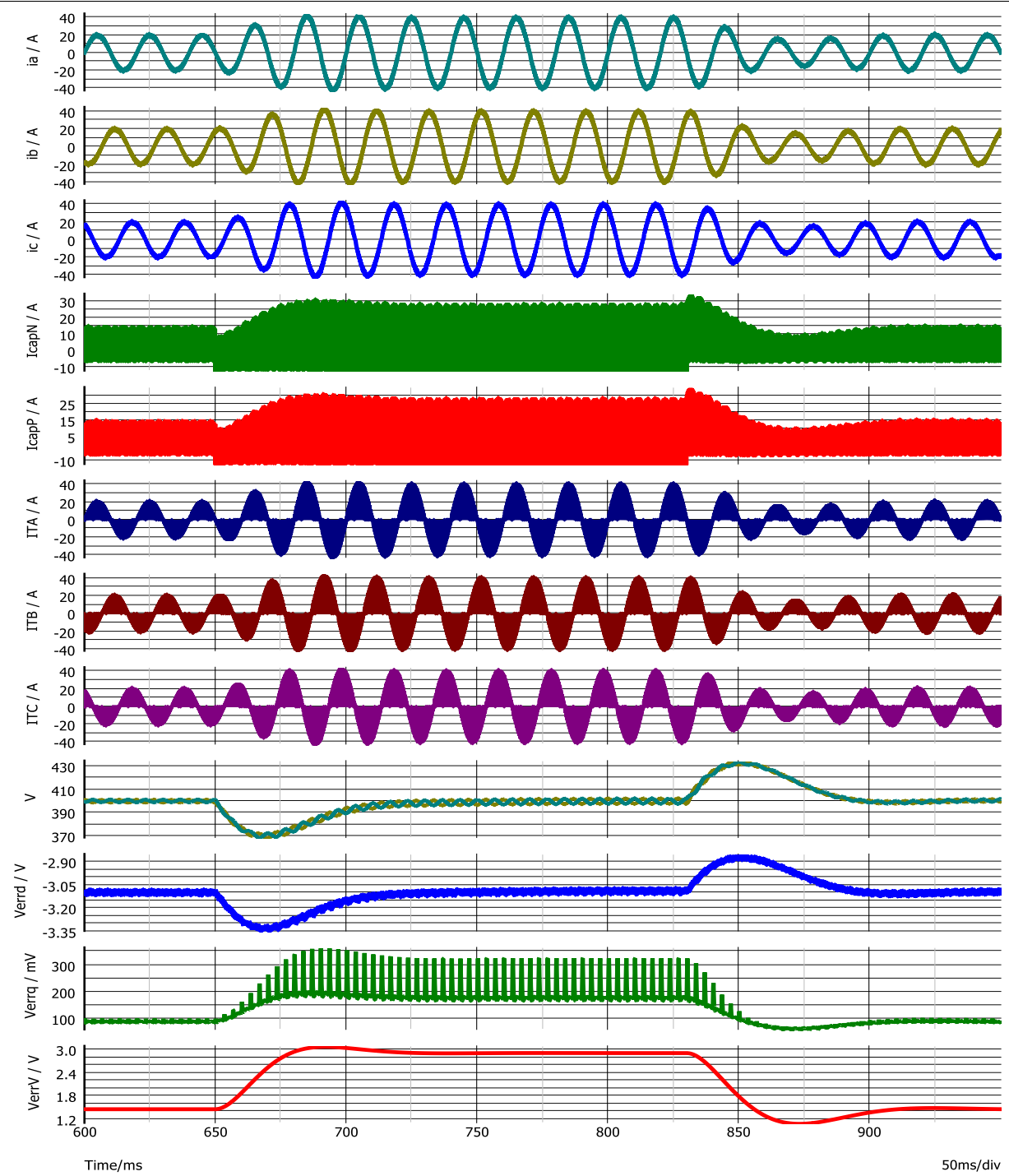
In theory, the d and q loops have the same ac response but changes can occur due to the dc loop kept closed during the ac sweep.

Curve label	Name	Value
Gain (...)	Gain Crossover Frequency	1.8637823kHz
Gain (...)	Gain Margin	***ERROR***
Phase ...	Phase Margin	63.379129degrees

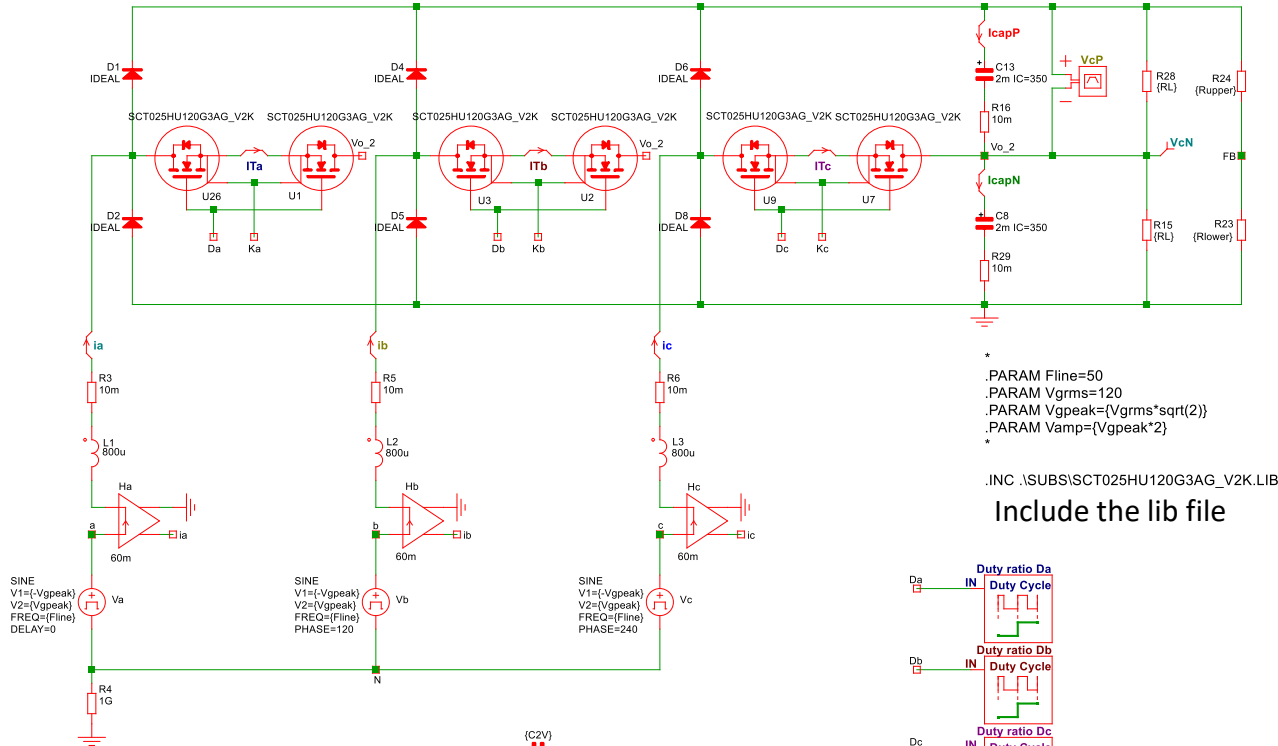


New cycle-by-cycle test – all clear!

The step load response is good, with a nice recovery.



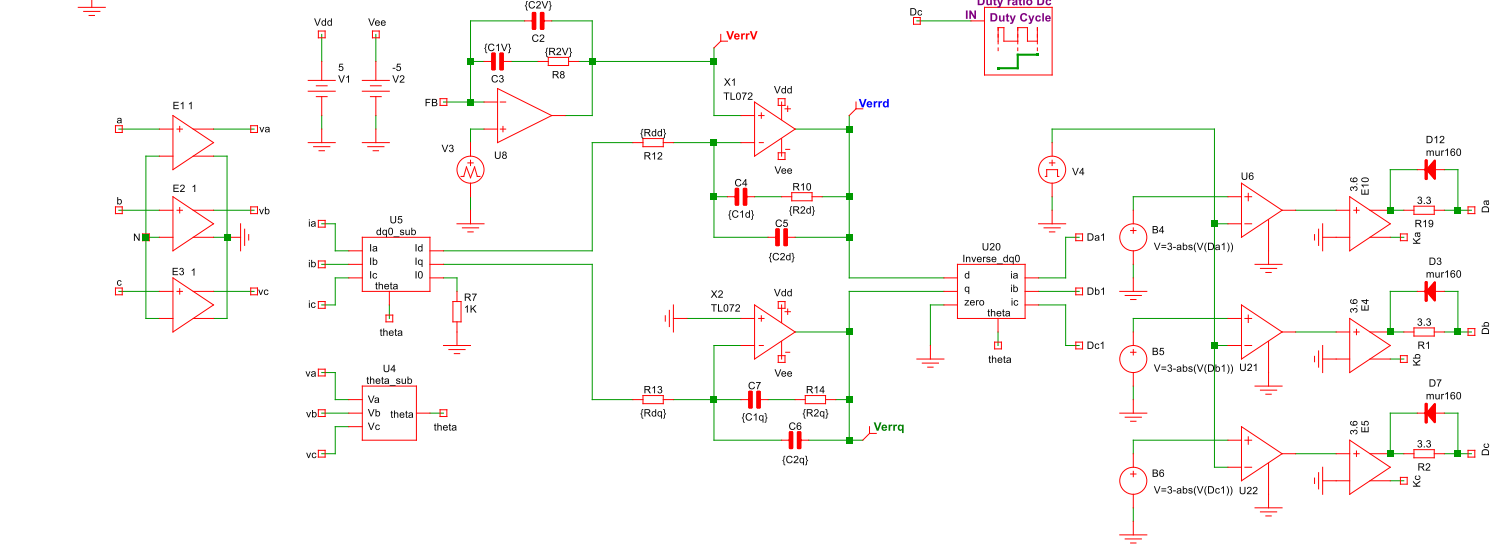
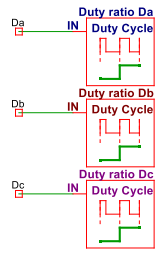
# Finally, I have included SiC MOSFETs in the circuit:



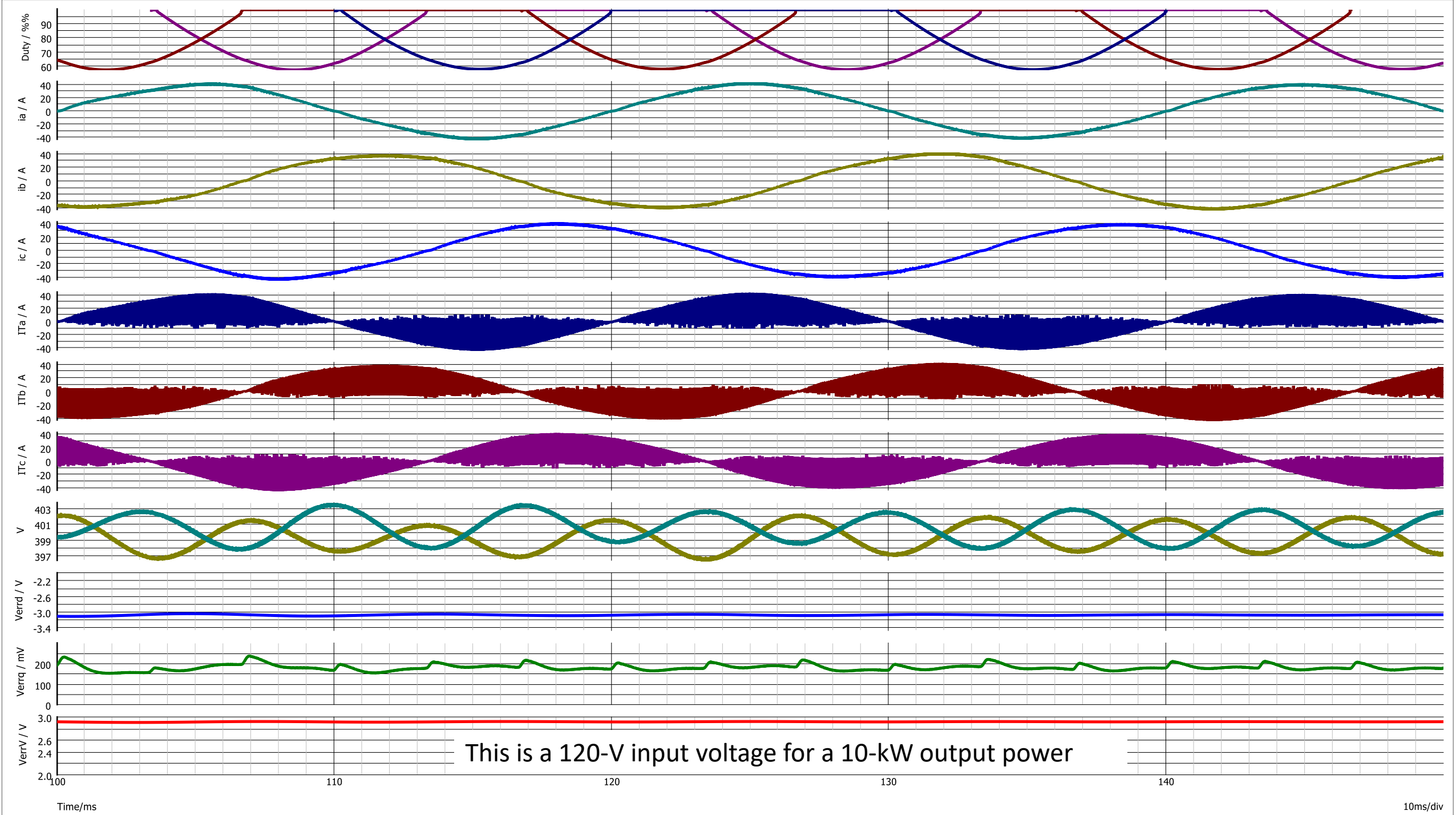
```
.param GfcV=32 ; magnitude at crossover *
.param PSV=45 ; phase lag at crossover *
* Enter Design Goals Information Here *
*
.param fcV=20 ; targeted crossover *
.param PMV=46 ; choose phase margin at crossover *
* Enter the Values for Vout and Bridge Bias Current *
*
.param Vout=800
.param Pout=10k ; nominal is 5 kW
.param RL=((Vout/2)^2/(Pout/2))
.param Ibias=100u
.param Vref=2.5
.param Rlower=(Vref/Ibias)
.param Rupper=((Vout-Vref)/Ibias)
* Do not edit the below lines *
.param boostV=(PMV-PSV-90)
.param GV=(10^(boostV/20))
.param kV=(tan((boostV/2+45)*pi/180))
.param fpV={fcV*kV}
.param fzV={fcV/kV}
.param C2V={1/(2*pi*fcV*GV*kV*Rupper)}
.param C1V={C2V*(kV^2-1)}
.param R2V={kV/(C1V*2*pi*fcV)}
* Choose op amp characteristics *
.param AOL=90 ; open-loop gain in dB *
.param POLE=30 ; low-frequency pole *
.param VHIGH=5 ; upper output level *
.param VLOW=100m ; lower output level *
* Do not edit these lines *
.param gm=100u
.param GAIN={10^(AOL/20)}
.param COL={1/(6.28*(GAIN/100u)*POLE)}
.param ROL={GAIN/100u}
```

```
* Components for the d loop *
.param Gfd=30 ; magnitude at crossover *
.param PSD=-93 ; phase lag at crossover *
* Enter Design Goals Information Here *
*
.param fcd=2k ; targeted crossover *
.param PMd=60 ; choose phase margin at crossover *
* Enter the Values for Vout and Bridge Bias Current *
*
.param Rdd=100k
* Do not edit the below lines *
.param boostd=(PMd-PSd-90)
.param Gd=(10^(boostd/20))
.param kd={tan((boostd/2+45)*pi/180)}
.param fpd={fcd*kd}
.param fzd={fcd/kd}
.param C2d=(1/(2*pi*fcd*Gd*kd*Rdd))
.param C1d=(C2d*(kd^2-1))
.param R2d={kd/(C1d*2*pi*fcd)}
* Components for the q loop *
.param Gfq=10 ; magnitude at crossover *
.param PSq=-93 ; phase lag at crossover *
* Enter Design Goals Information Here *
*
.param fcq=2k ; targeted crossover *
.param PMq=60 ; choose phase margin at crossover *
*
.param Rdq=100k
* Do not edit the below lines *
.param boostq=(PMq-PSq-90)
.param Gq=(10^(boostq/20))
.param kq={tan((boostq/2+45)*pi/180)}
.param fpq={fcq*kq}
.param fzq={fcq/kq}
.param C2q=(1/(2*pi*fcq*Gq*kq*Rdq))
.param C1q=(C2q*(kq^2-1))
.param R2q={kq/(C1q*2*pi*fcq)}
```

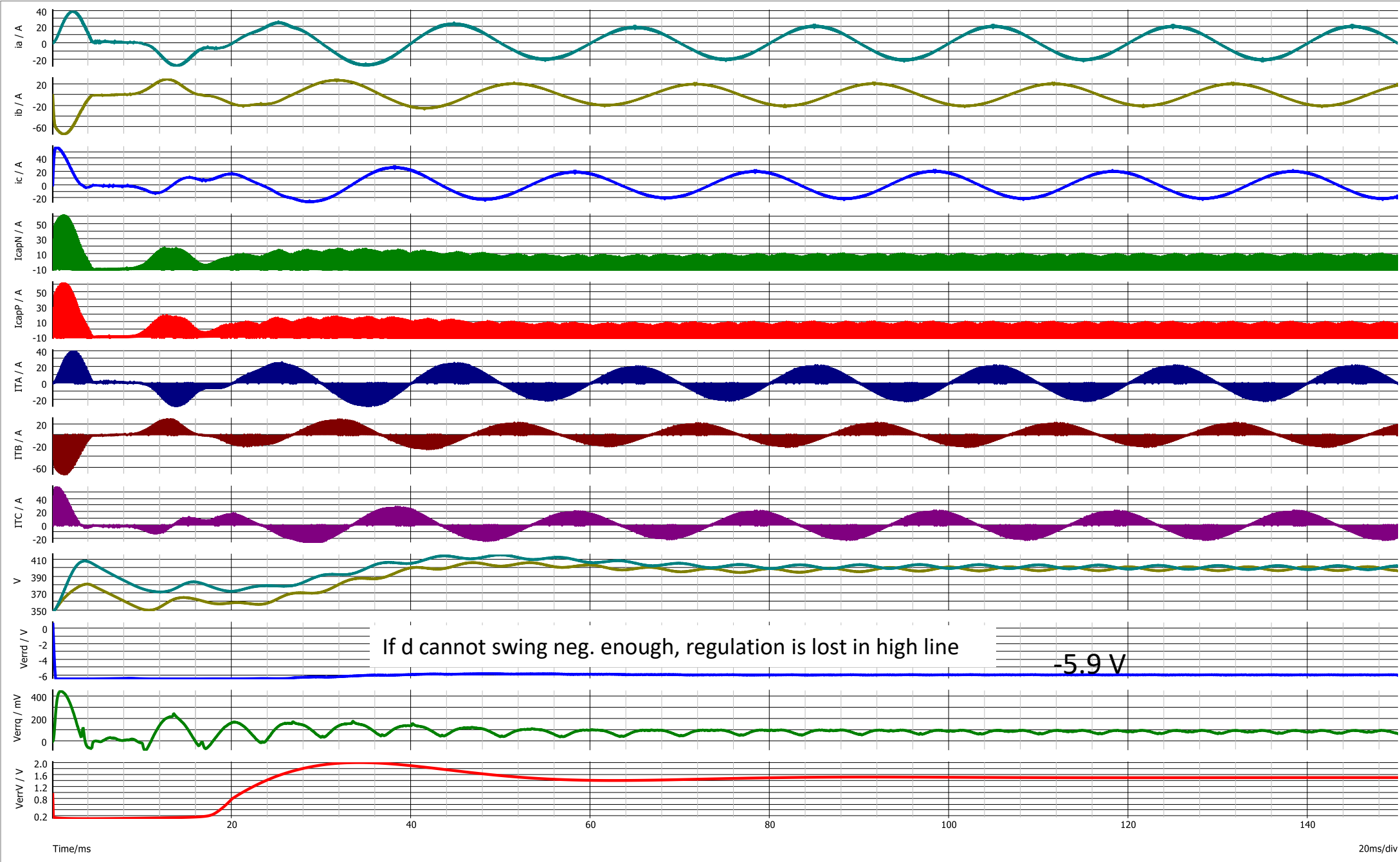
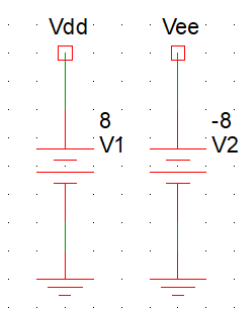
\*  
 .PARAM Fline=50  
 .PARAM Vgrms=120  
 .PARAM Vgpeak=(Vgrms\*sqrt(2))  
 .PARAM Vamp=(Vgpeak\*2)  
 \*  
 .INC \SUBS\SCT025HU120G3AG\_V2K.LIB  
 Include the lib file



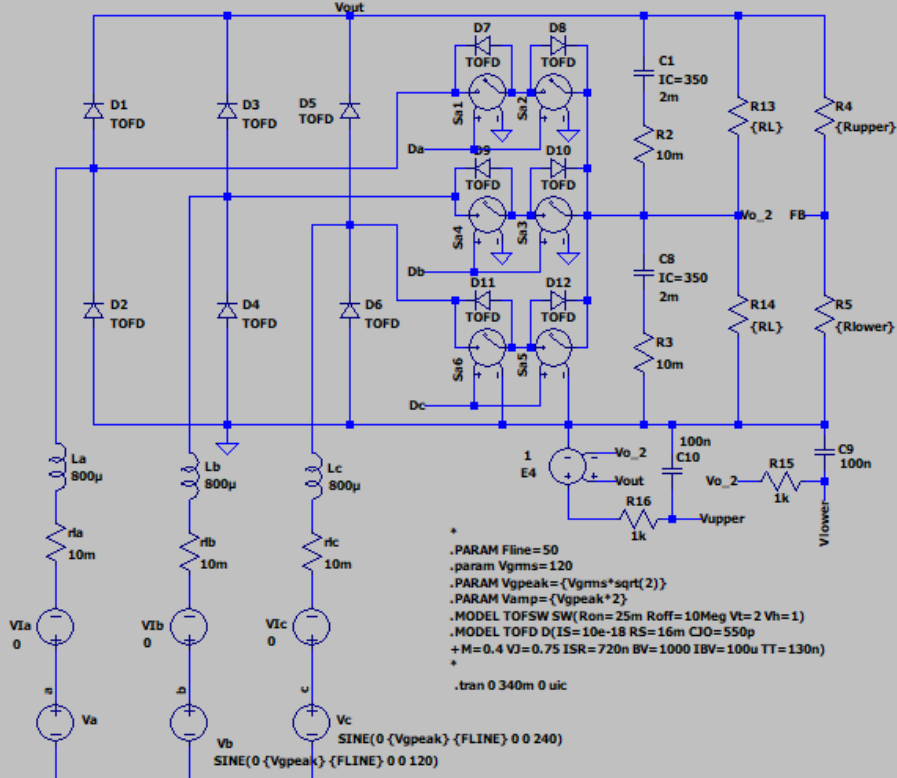
The simulation with SiC transistors is the final step. The driver side is simplified and delivers up to 18 V through a 3.3-Ω resistance. A more accurate simulation should include a comprehensive model of the driving path.



This is the high-line simulation (230 V rms line-neutral or 400 V line-to-line) and you can notice the d value swinging to almost -6 V. You need sufficient dc supplies on the op-amp, what I originally did not have with the +5/-5 V. I increased them to +8/-8 for this sim.



20ms/div



```

.options abstol=1u vntol=1m reitot=0.01 gmin=100p
+method=gear

.four 50 10 -1 I(Via)
.four 50 10 -1 I(Vib)
.four 50 10 -1 I(Vic)

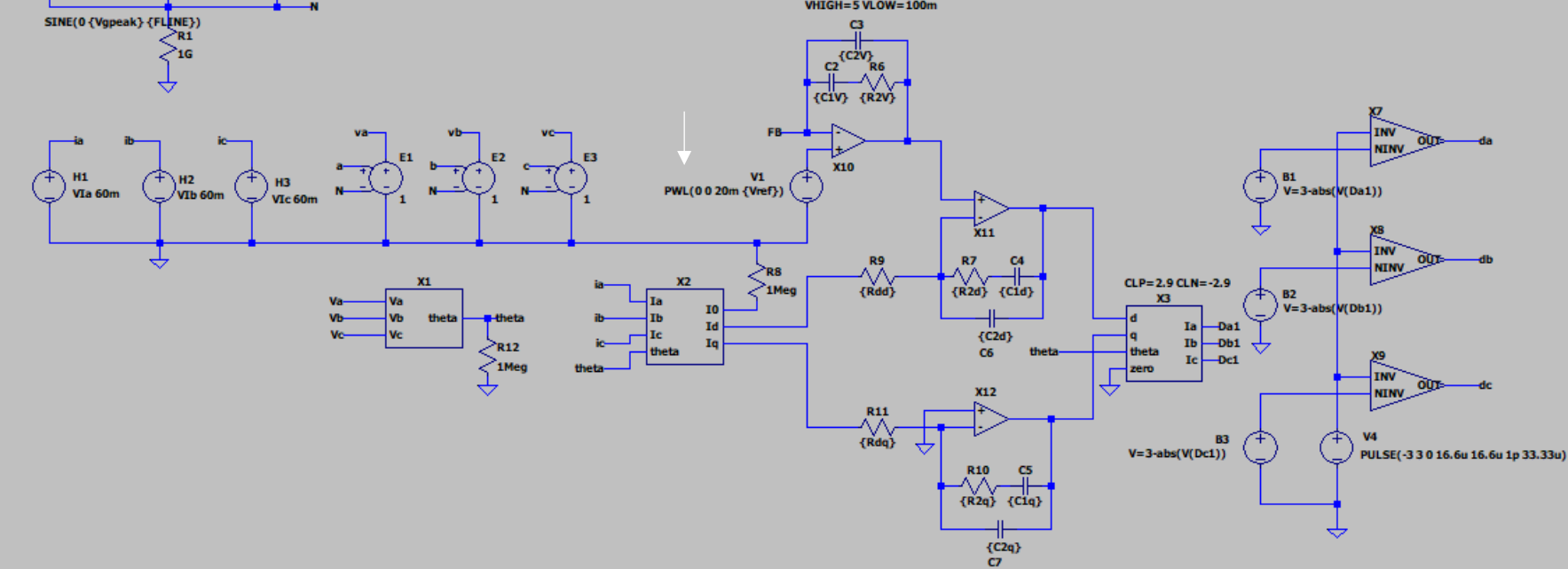
.param GfcV=35 ; magnitude at crossover +
.param PSV=-62 ; phase lag at crossover +
*
* Enter Design Goals Information Here +
*
.param fcV=10 ; targeted crossover +
.param PMV=60 ; choose phase margin at crossover +
*
* Enter the Values for Vout and Bridge Bias Current +
*
.param Rdd=100k
*
* Do not edit the below lines +
.param boostd=(PMd-PSd-90)
.param Gd={10**(-GfcV/20)}
.param kd={tan((boostd/2+45)*pi/180)}
.param fpd={fcd/kd}
.param C2d={1/(2*pi*fcd*Gd*kd*Rdd)}
.param C1d={C2d*(kd**2-1)}
.param R2d={kd/(C1d*2*pi*fcd)}
*
* Components for the q loop +
.param Gfcq=-1.2 ; magnitude at crossover +
.param PSq=-93 ; phase lag at crossover +
*
* Enter Design Goals Information Here +
*
.param fcq=1k ; targeted crossover +
.param PMq=60 ; choose phase margin at crossover +
*
.param Rdq=100k
*
* Do not edit the below lines +
.param boostq=(PMq-PSq-90)
.param Gq={10**(-Gfcq/20)}
.param kq={tan((boostq/2+45)*pi/180)}
.param fpq={fcq*kq}
.param C2q={1/(2*pi*fcq*Gq*kq*Rdq)}
.param C1q={C2d*(kq**2-1)}
.param R2q={kq/(C1q*2*pi*fcq)}

```

```

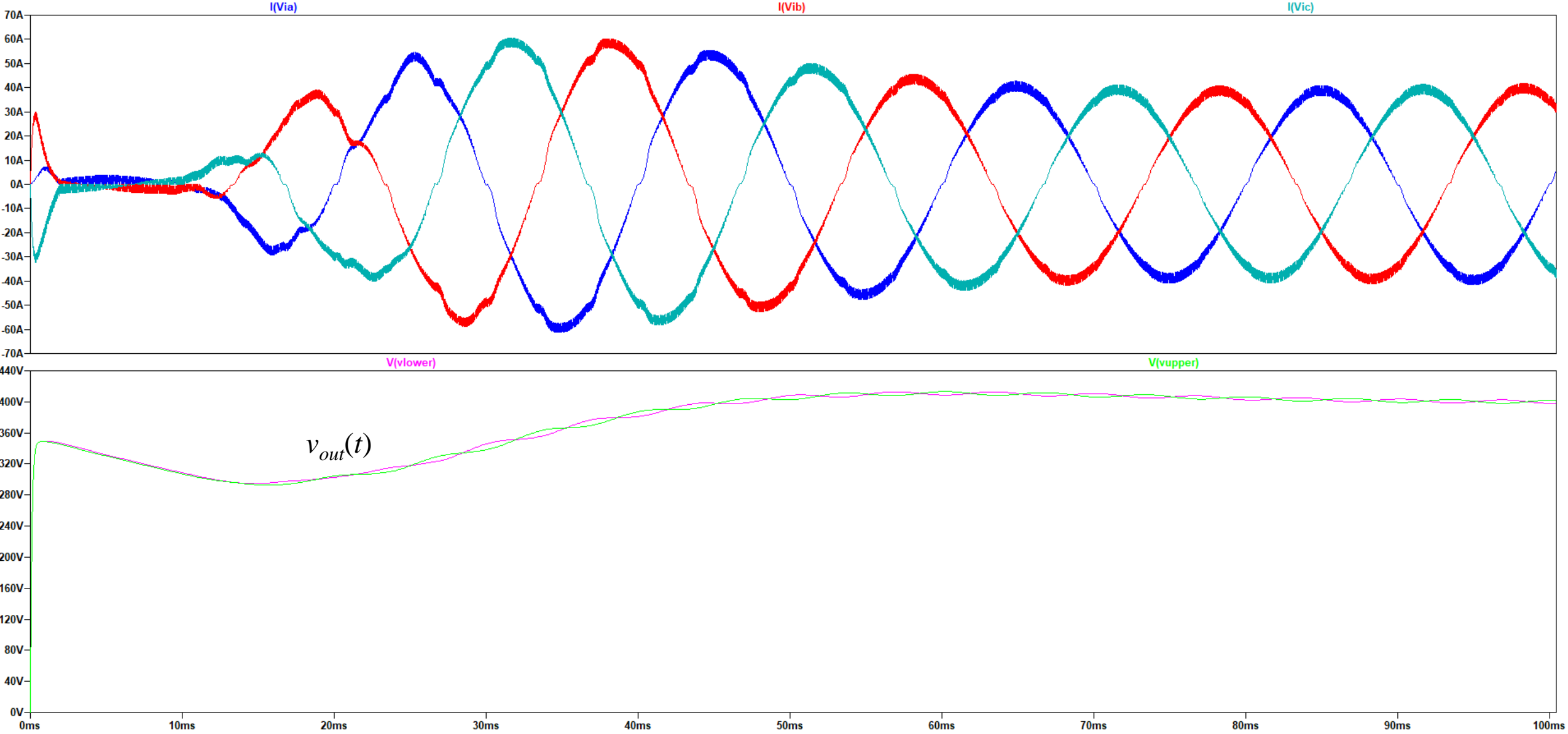
.PARAM Fline=50
.param Vgms=120
.PARAM Vgpeak={Vgms*sqrt(2)}
.PARAM Vamp={Vgpeak*2}
.MODEL TOFSW SW(Ron=25m Roff=10Meg Vt=2 Vh=1)
.MODEL TOFD D(IS=10e-18 RS=16m CJO=550p
+M=0.4 VJ=0.75 ISR=720n BV=1000 IBV=100u TT=130n)
*
.tran 0 340m 0 uic

```

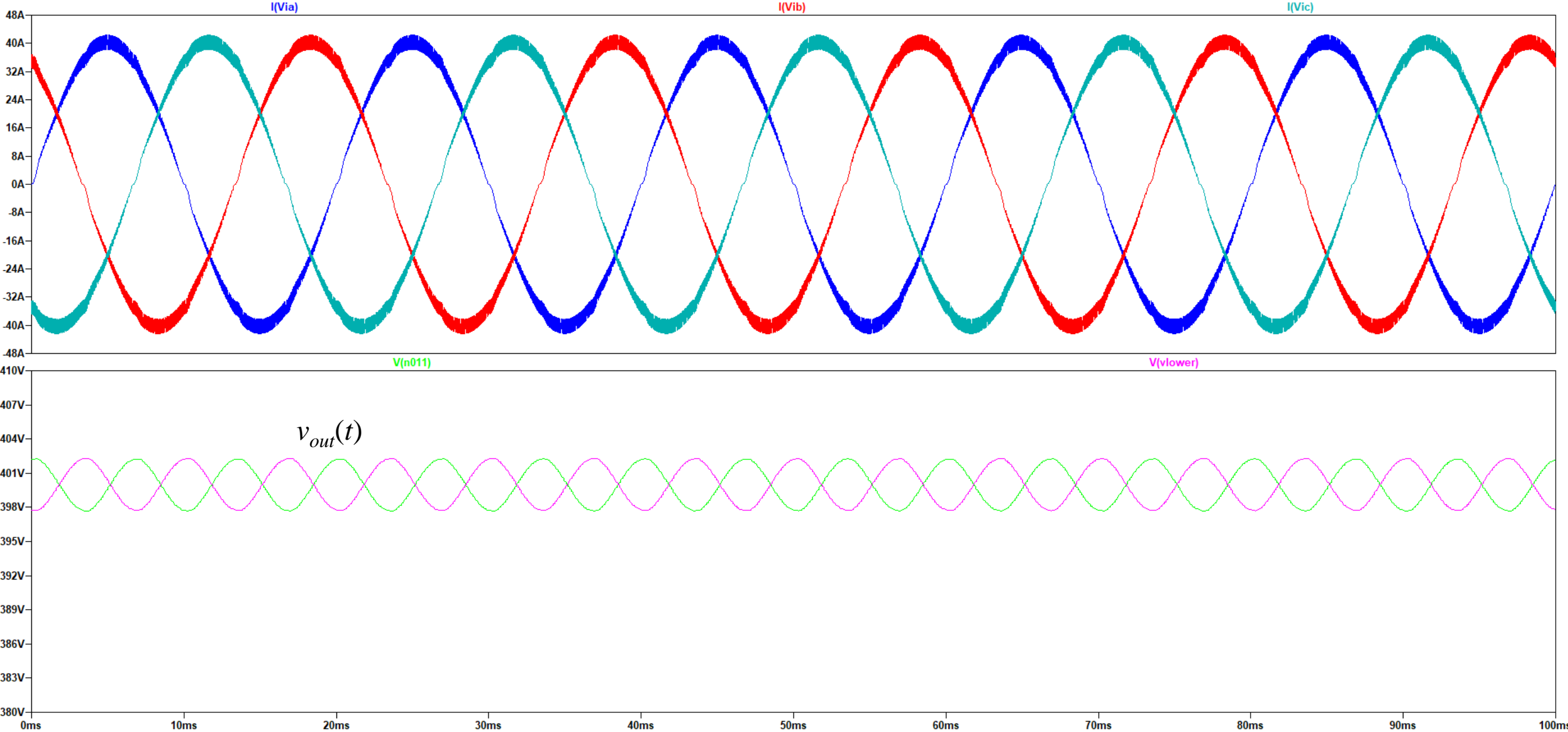


This is the cycle-by-cycle implementation in LTspice, reusing the dq blocks originally tested with the 6-pack PFC.

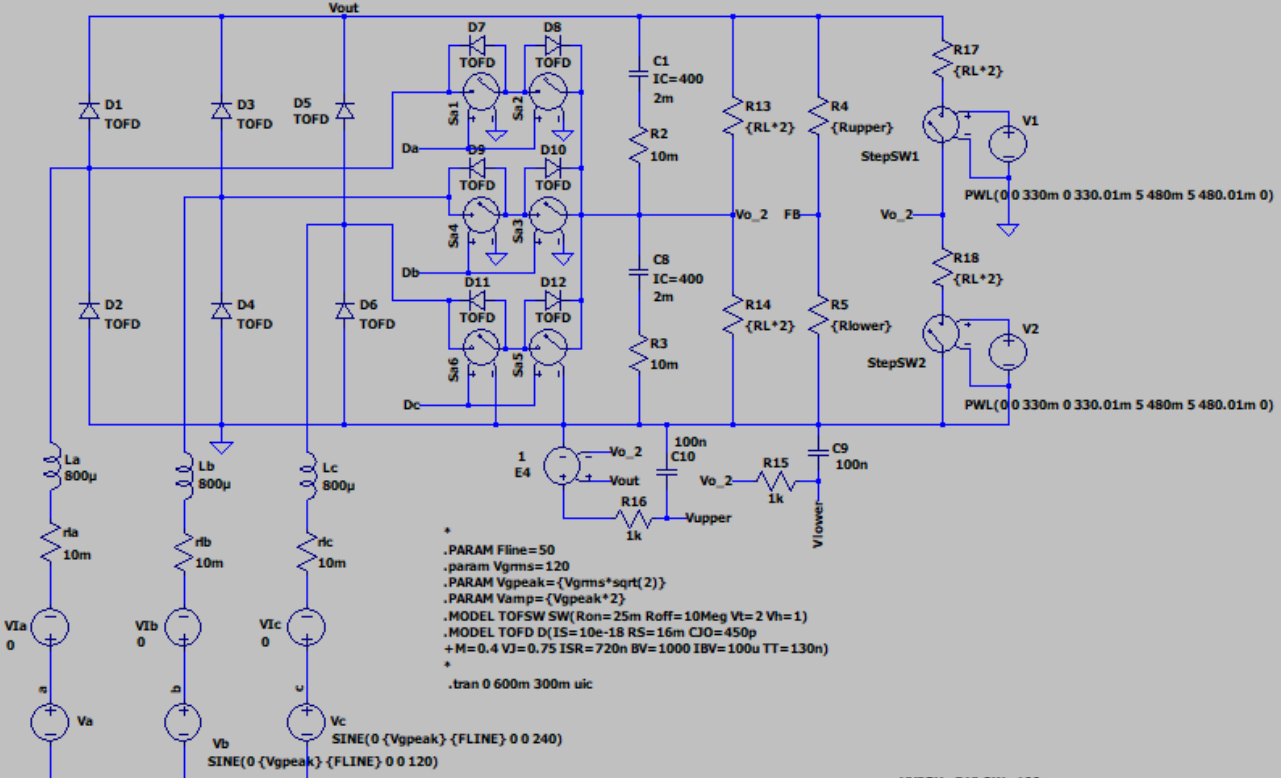
The reference voltage is soft-started for a smooth power-on sequence.



The input currents nicely grow to their nominal values after a few tens of milliseconds.



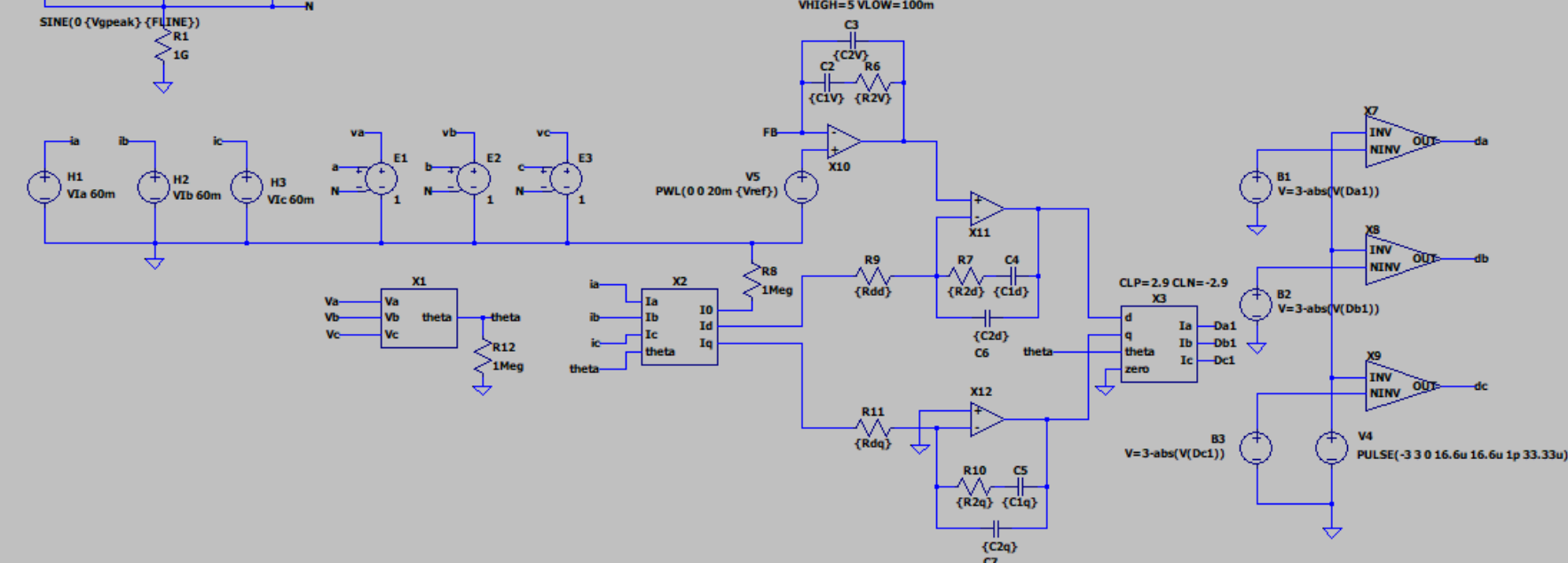
At steady-state, the input currents are well sinusoidal and the outputs are properly regulated.



```

.PARAM Fline=50
.param Vgrms=120
.PARAM Vgpeak={Vgrms*sqrt(2)}
.PARAM Vamp={Vgpeak*2}
.MODEL TOFSW SW(Ron=25m Roff=10Meg Vt=2 Vh=1)
.MODEL TOFD D(IS=10e-18 RS=16m CJO=450p
+M=0.4 VJ=0.75 ISR=720n BV=1000 IBV=100u TT=130n)
.tran 0 600m 300m uic

```

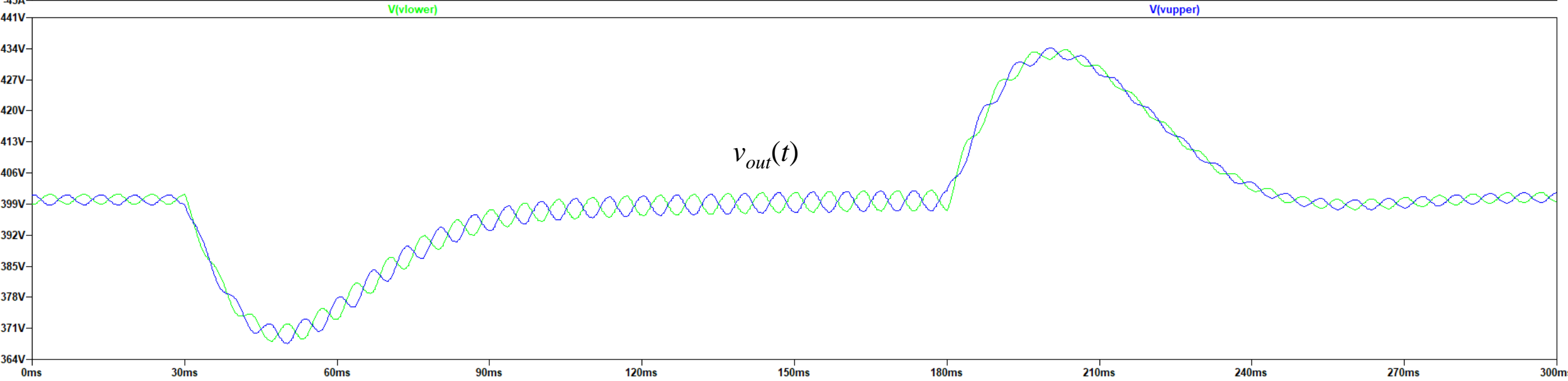
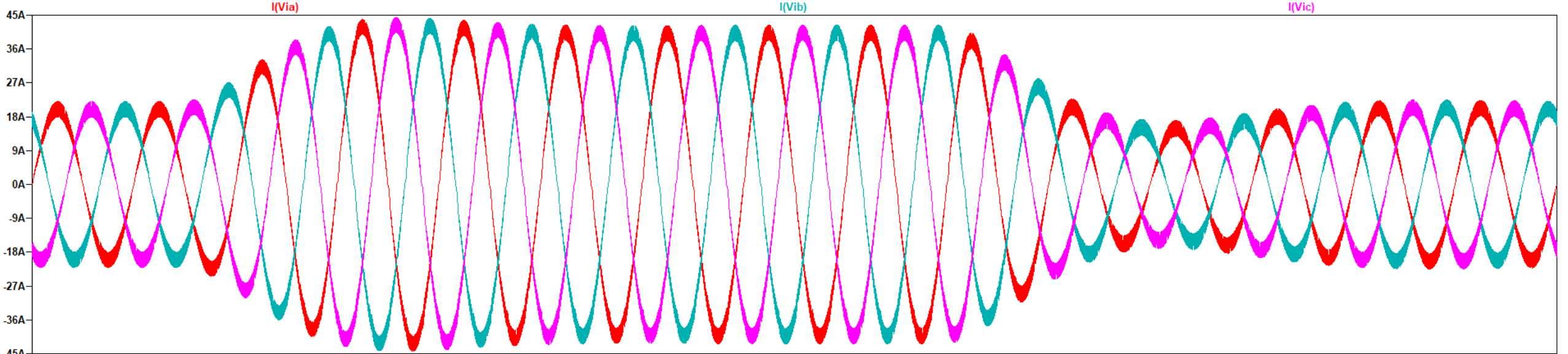


```

.options abstol=1u vntol=1m reitol=0.01 gmin=100p
+method=gear
.param Gfcd=-1.2 ; magnitude at crossover *
.param PSd=-93 ; phase lag at crossover *
* Enter Design Goals Information Here *
*
.param fcd=1k ; targeted crossover *
.param PMd=60 ; choose phase margin at crossover *
* Enter the Values for Vout and Bridge Bias Current *
*
.param Rdd=100k
* Do not edit the below lines *
.param boostd={PMd-PSd-90}
.param Gd={10**(-Gfcd/20)}
.param kd={tan((boostd/2+45)*pi/180)}
.param fpd={fcd*kd}
.param fad={fcd/kd}
.param C2d={1/(2*pi*fcd*Gd*kd*Rdd)}
.param C1d={C2d*(kd**2-1)}
.param R2d={kd/(C1d*2*pi*fcd)}
* Components for the q loop *
.param Gfcq=-1.2 ; magnitude at crossover *
.param PSq=-93 ; phase lag at crossover *
* Enter Design Goals Information Here *
*
.param fcq=1k ; targeted crossover *
.param PMq=60 ; choose phase margin at crossover *
*
.param Rdq=100k
* Do not edit the below lines *
.param boostq={PMq-PSq-90}
.param Gq={10**(-Gfcq/20)}
.param kq={tan((boostq/2+45)*pi/180)}
.param fpq={fcq*kq}
.param fqq={fcq/kq}
.param C2q={1/(2*pi*fcq*Gq*kq*Rdq)}
.param C1q={C2q*(kq**2-1)}
.param R2q={kq/(C1q*2*pi*fcq)}

```

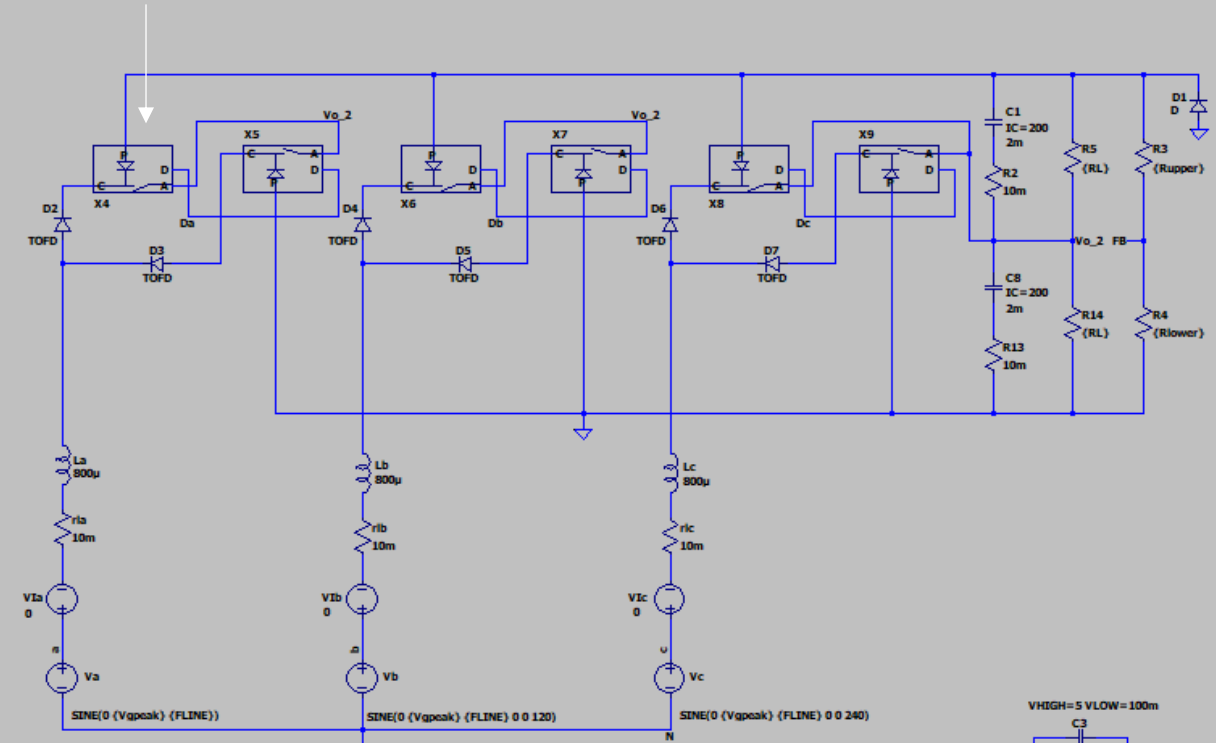
In this simulation, the load is stepped from 50% to 100% on each of the output rails.



The output response is stable, with a good recovery.

# The VM PWM switch

This is the averaged model of the Vienna rectifier. The key here is, again, to soft-start the reference voltage.

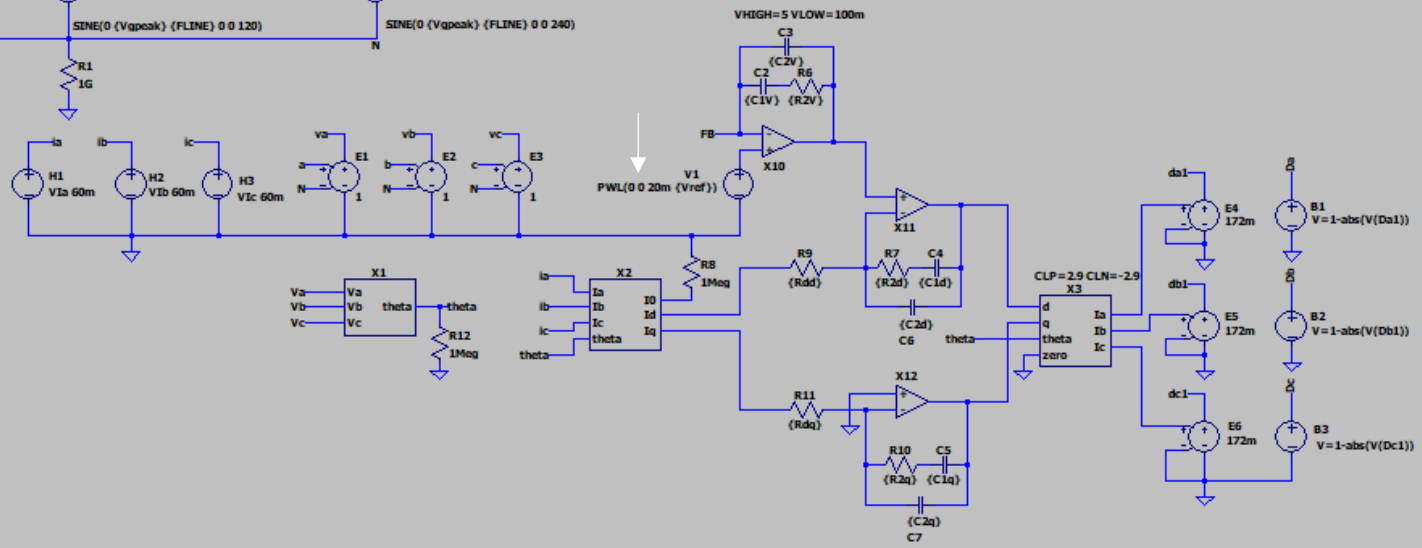


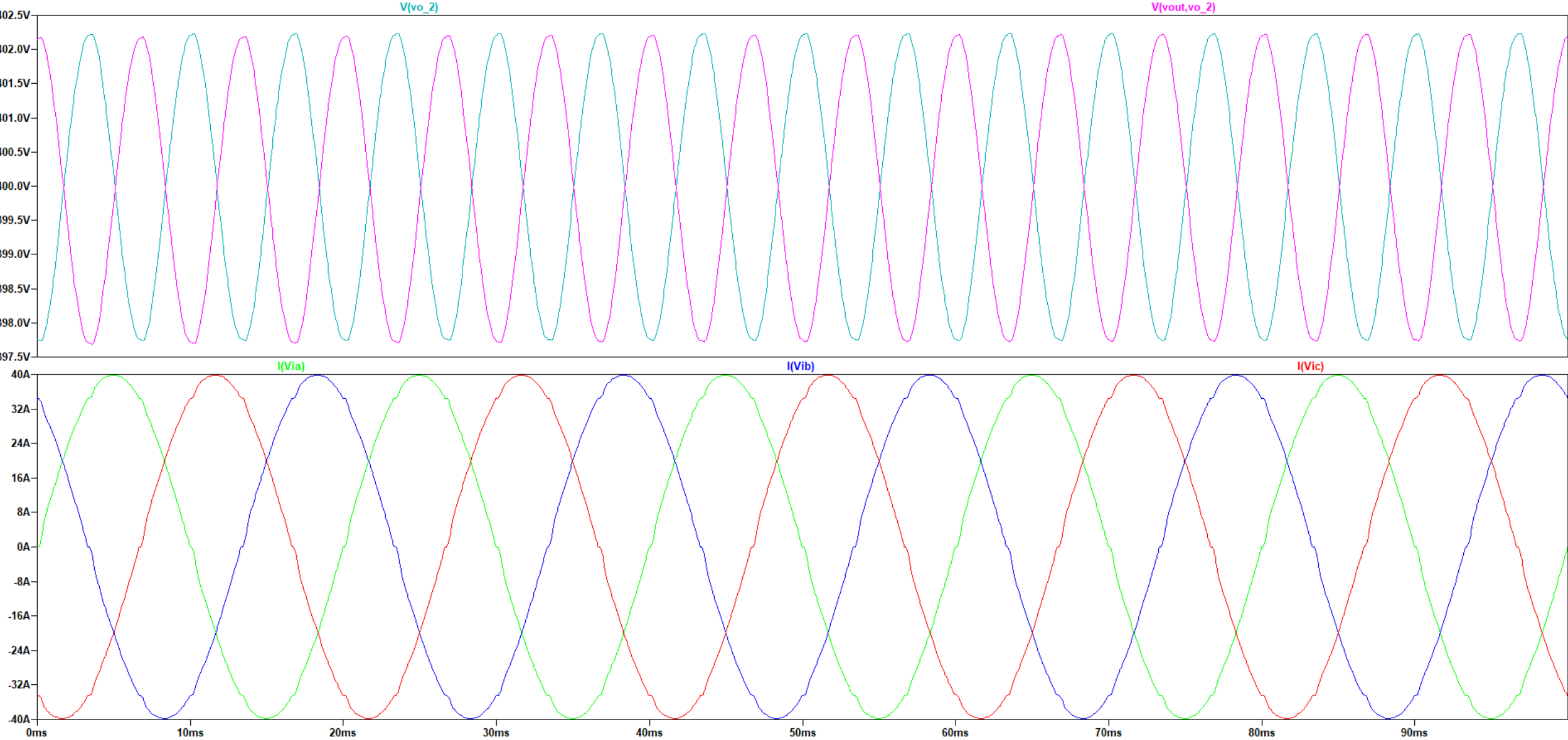
```

.tran 0 300m 200m uic

.four 50 10 -1 I(Via)
.four 50 10 -1 I(Vib)
.four 50 10 -1 I(Vic)
*
.PARAM Fline=50
.PARAM Vgrms=120
.PARAM Vvpeak=(Vgrms*sqrt(2))
.PARAM Vvamp=(Vvpeak*2)
.MODEL TOFSW SW(Ron=25m Roff=10Meg Vt=2 Vh=1)
.MODEL TOFD DI(S=10e-15 RS=16m CJO=500p
+M=0.4 VJ=0.75 ISR=720n BV=1000 IBV=100u TT=130n)
*
* Components for the d loop *
.param Gfcd=-1.2; magnitude at crossover *
.param PSd=-93; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fcd=1k; targeted crossover *
.param PMd=60; choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Rdd=100k
*
* Do not edit the below lines *
.param boostd=(PMd-PSd-90)
.param Gd=(10**(-Gfcd/20))
.param kd=(tan(boostd/2+45)*pi/180)
.param fzd=(fcd/kd)
.param C2d=(1/(2*pi*fcd*Gd*kd*Rdd))
.param C1d=(C2d*(kd**2-1))
.param R2d=(kd/(C1d*2*pi*fcd))
*
* Components for the q loop *
.param Gfcq=-1.2; magnitude at crossover *
.param PSq=-93; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fcq=1k; targeted crossover *
.param PMq=60; choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Rdq=100k
*
* Do not edit the below lines *
.param boostq=(PMq-PSq-90)
.param boostq=(PMq-PSq-90)
.param Gq=(10**(-Gfcq/20))
.param kd=(tan(boostq/2+45)*pi/180)
.param fzd=(fcd/kd)
.param C2q=(1/(2*pi*fcd*Gq*kd*Rdq))
.param C1q=(C2q*(kd**2-1))
.param R2q=(kd/(C1q*2*pi*fcd))
*

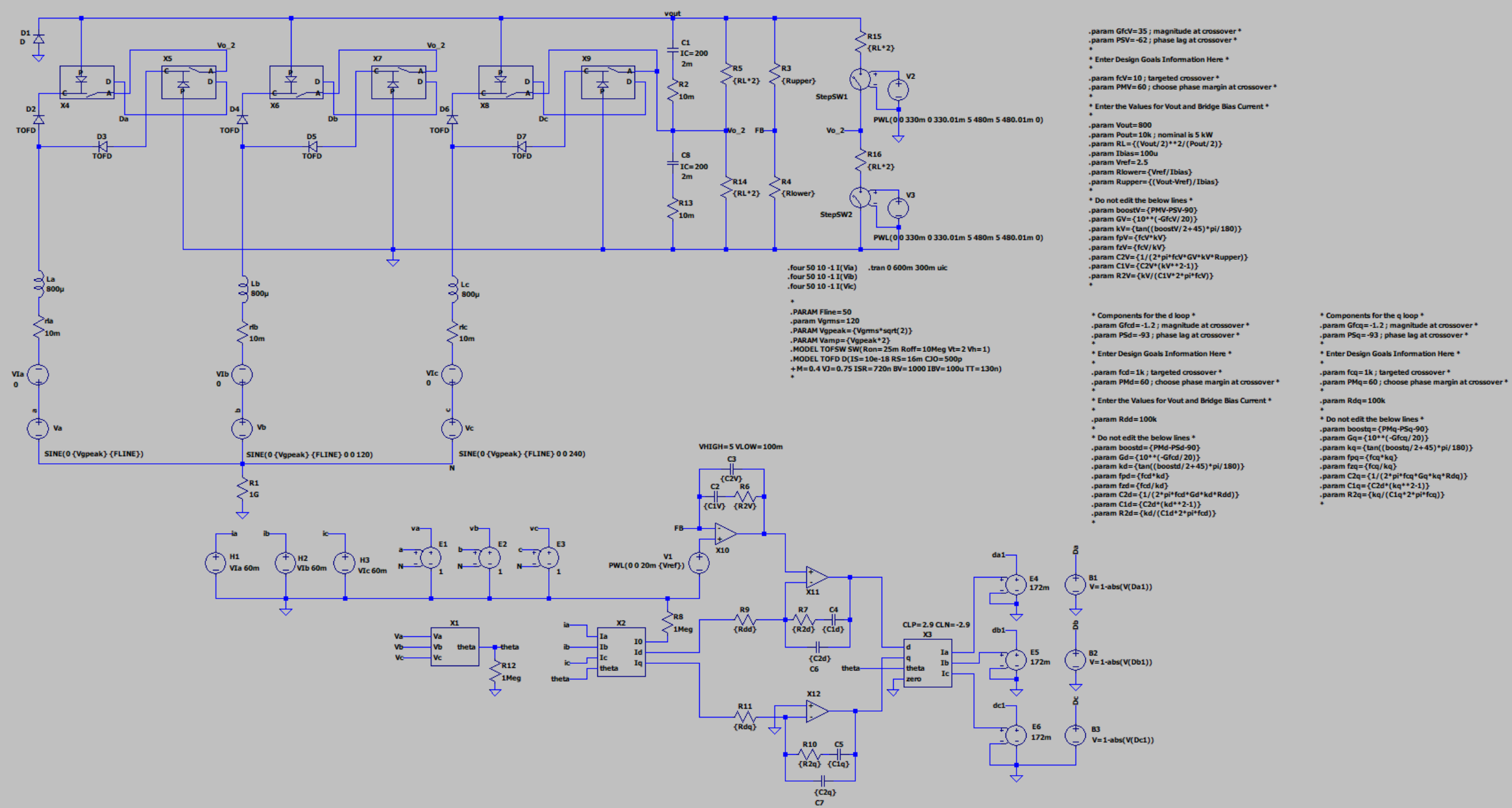
```



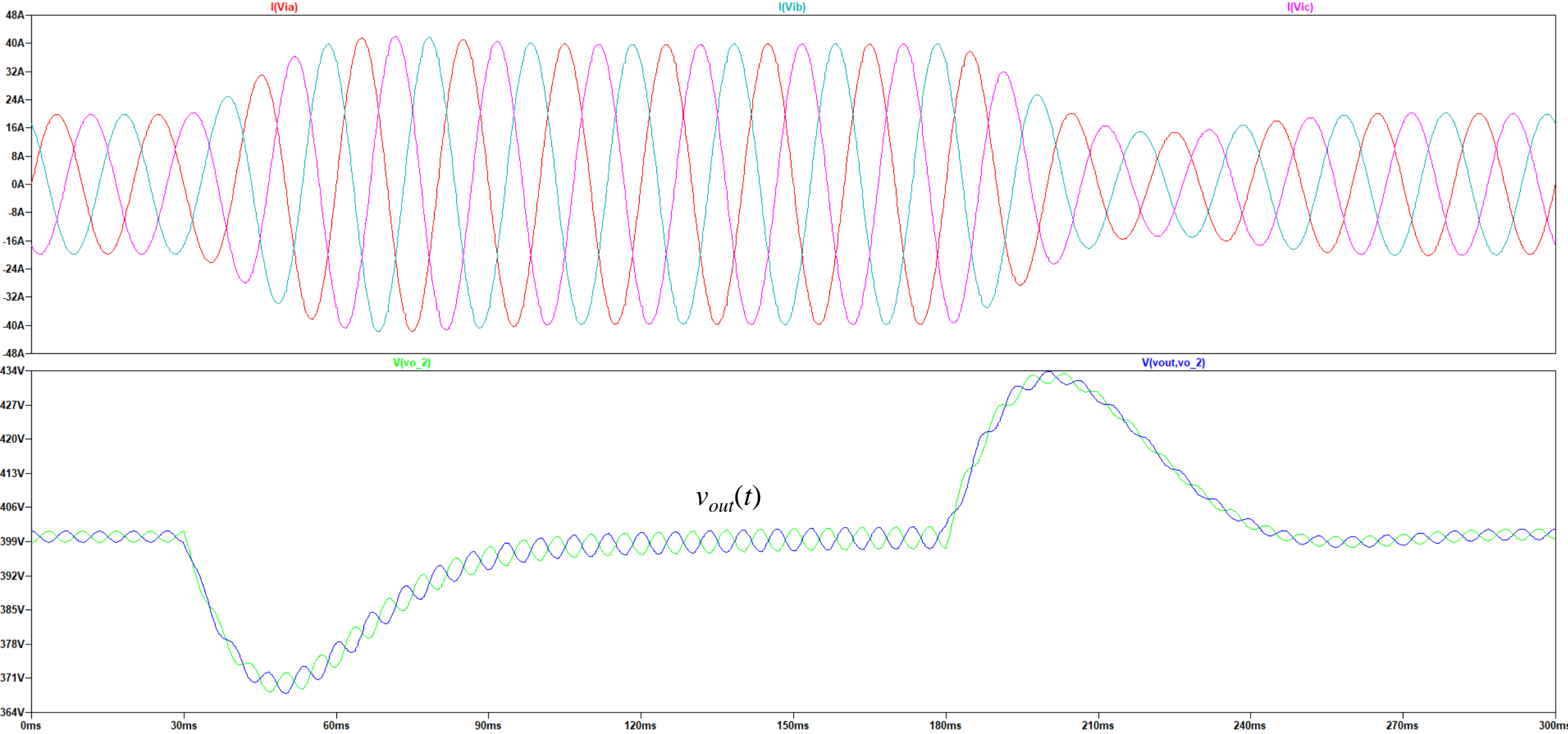


The input currents are nicely sinusoidal and both output rails are regulated at 400 V

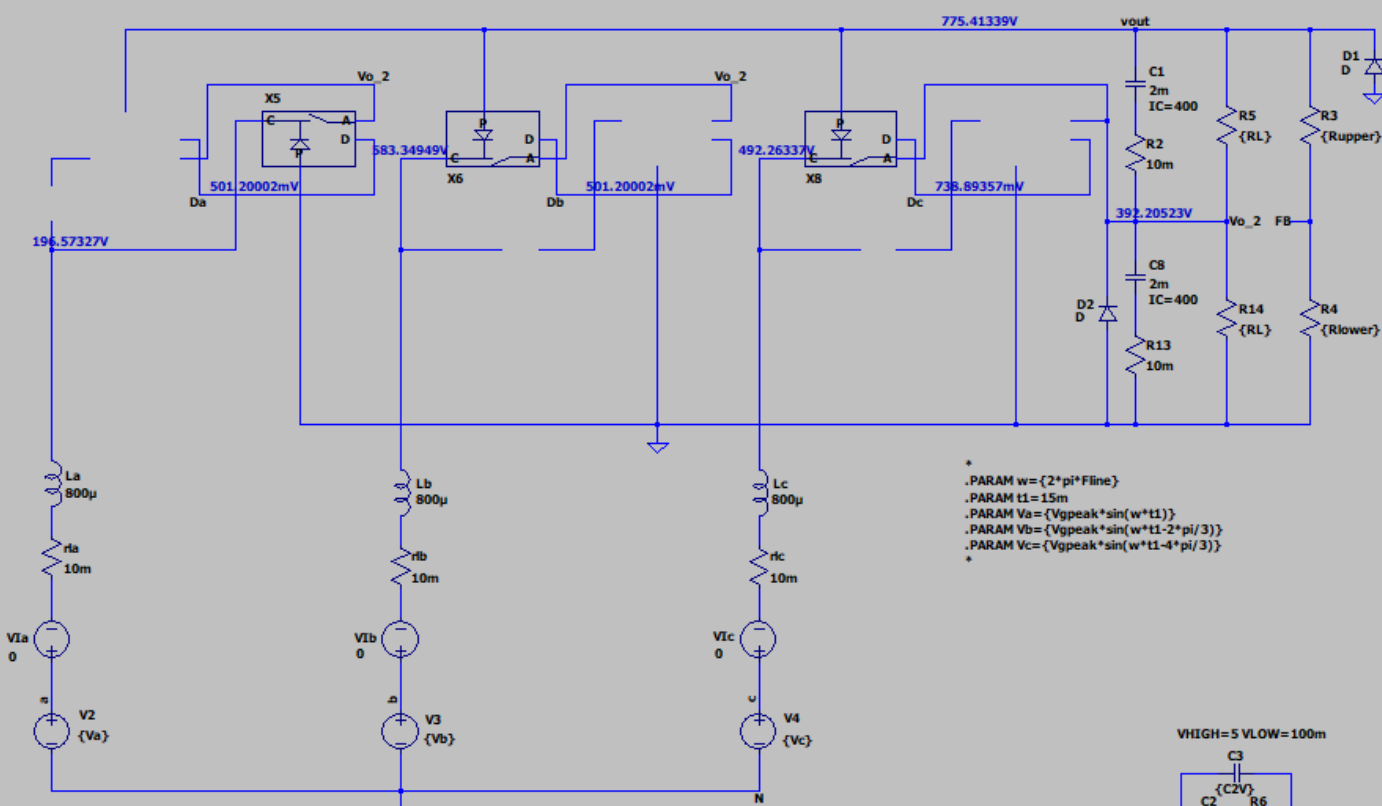
$V_{in} = 120 \text{ V rms}$ ,  $P_{out} = 10 \text{ kW}$



This is template for the load transient response in averaged mode.



This is the response to a load step, from 5 to 10 kW. Excellent match with the cycle-by-cycle version.



.ac dec 100 1 10k

```

*
.PARAM Fline=50
.PARAM Vgrms=120
.PARAM Vgpeak={Vgrms*sqrt(2)}
.PARAM Vamp={Vgpeak*2}
*
* Enter Design Goals Information Here *
*
.PARAM GfcV=35 ; magnitude at crossover +
.PARAM PSV=-62 ; phase lag at crossover +
*
* Enter Design Goals Information Here *
*
.PARAM fcv=10 ; targeted crossover +
.PARAM PMV=60 ; choose phase margin at crossover +
*
* Enter the Values for Vout and Bridge Bias Current +
*
.PARAM Vout=800
.PARAM Pout=10k ; nominal is 5 kW
.PARAM RL={{(Vout/2)**2/(Pout/2)}}
.PARAM Ibias=100u
.PARAM Vref=2.5
.PARAM Rlower={Vref/Ibias}
.PARAM Rupper={{(Vout-Vref)/Ibias}}
*
* Do not edit the below lines +
.PARAM boostV={PMV-PSV-90}
.PARAM GV={10**(-GfcV/20)}
.PARAM kV={tan((boostV/2+45)*pi/180)}
.PARAM fV={fcv*kV}
.PARAM C2V={1/(2*pi*fV*GV*kV*Rupper)}
.PARAM C1V={C2V*(kV**2-1)}
.PARAM R2V={kV/(C1V*2*pi*fV)}
*

```

```

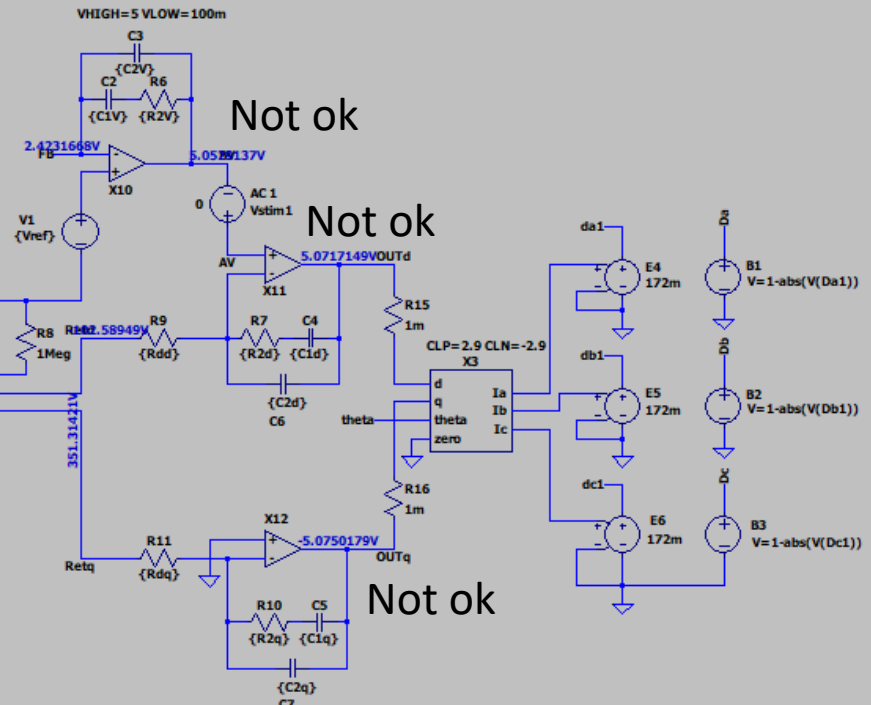
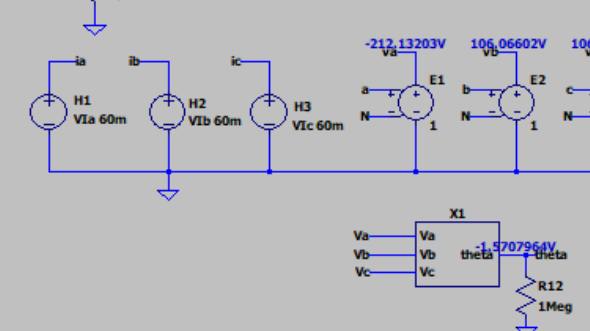
* Components for the d loop +
.PARAM Gfcd=-1.2 ; magnitude at crossover +
.PARAM PSd=-93 ; phase lag at crossover +
*
* Enter Design Goals Information Here +
*
.PARAM fcd=1k ; targeted crossover +
.PARAM PMd=60 ; choose phase margin at crossover +
*
* Enter the Values for Vout and Bridge Bias Current +
*
.PARAM Rdd=100k
*
* Do not edit the below lines +
.PARAM boostd={PMd-PSd-90}
.PARAM Gd={10**(-Gfcd/20)}
.PARAM kd={tan((boostd/2+45)*pi/180)}
.PARAM fpd={fcd*kd}
.PARAM fzd={fcd/kd}
.PARAM C2d={1/(2*pi*fpd*Gd*kd*Rdd)}
.PARAM C1d={C2d*(kd**2-1)}
.PARAM R2d={kd/(C1d*2*pi*fcd)}
*
* Components for the q loop +
.PARAM Gfcq=-1.2 ; magnitude at crossover +
.PARAM PSq=-93 ; phase lag at crossover +
*
* Enter Design Goals Information Here +
*
.PARAM fcq=1k ; targeted crossover +
.PARAM PMq=60 ; choose phase margin at crossover +
*
* Do not edit the below lines +
.PARAM boostq={PMq-PSq-90}
.PARAM Gq={10**(-Gfcq/20)}
.PARAM kq={tan((boostq/2+45)*pi/180)}
.PARAM fcq={fcq*kq}
.PARAM fzq={fcq/kq}
.PARAM C2q={1/(2*pi*fcq*Gq*kq*Rdq)}
.PARAM C1q={C2d*(kq**2-1)}
.PARAM R2q={kq/(C1q*2*pi*fcq)}
*

```

```

*
.PARAM w={2*pi*Fline}
.PARAM tL=15m
.PARAM Va={Vgpeak*sin(w*tL)}
.PARAM Vb={Vgpeak*sin(w*tL-2*pi/3)}
.PARAM Vc={Vgpeak*sin(w*tL-4*pi/3)}
*

```

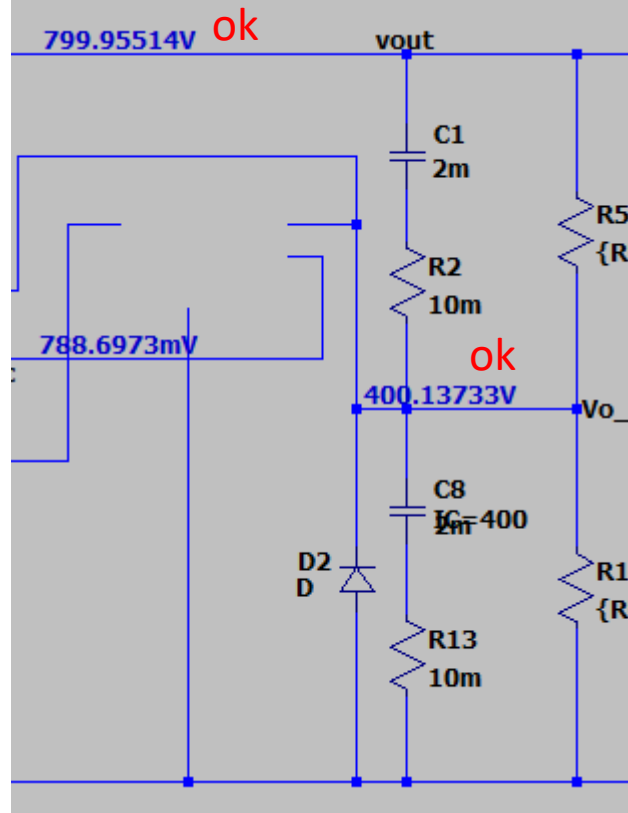
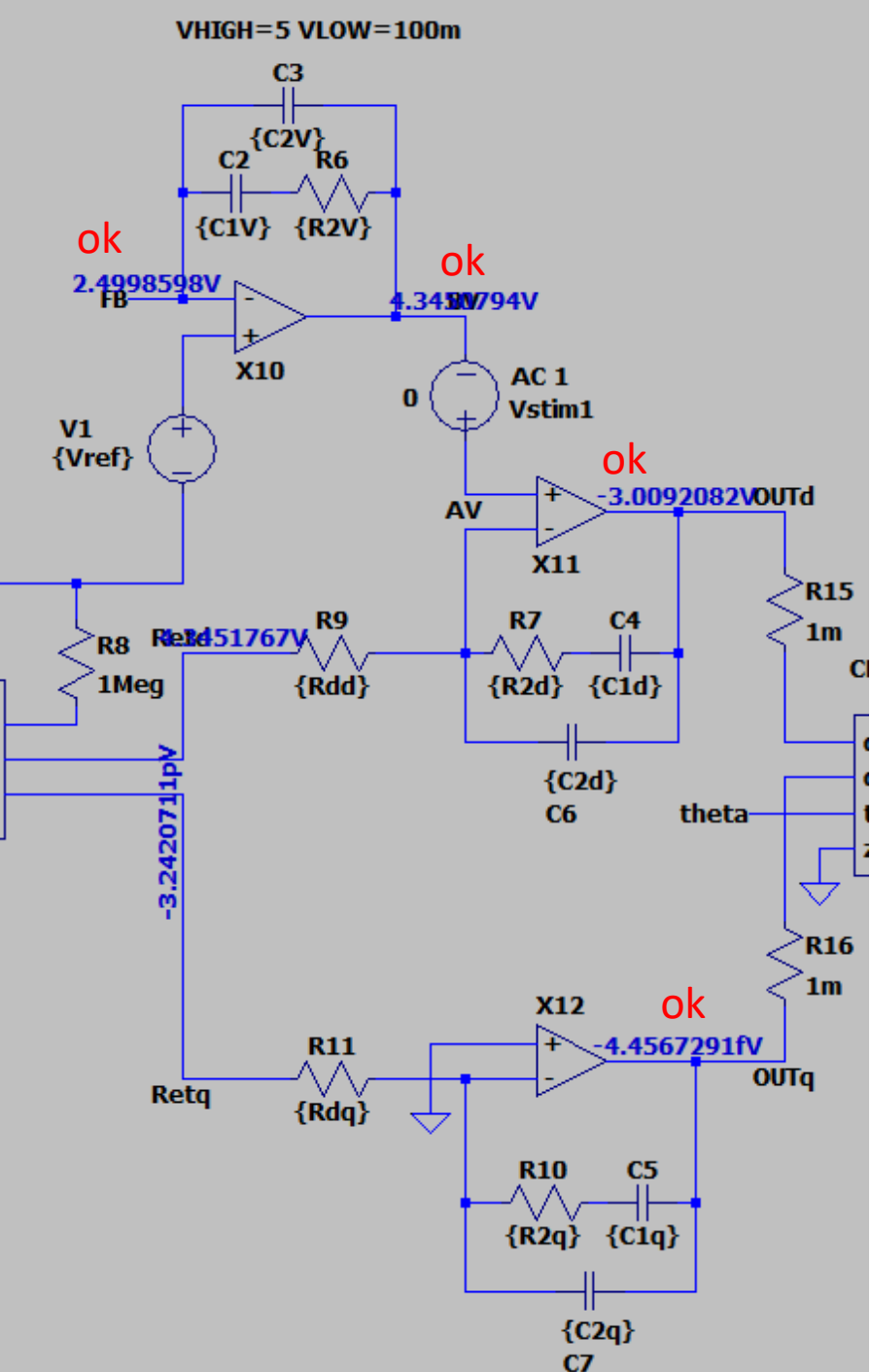


Not ok

Not ok

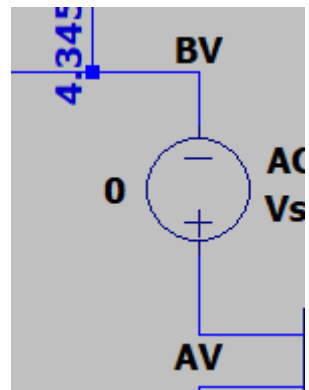
Not ok

The operating point is wrong and I could not find a way to have it converging to the correct value despite changing the .IC values or clamping sources. Until I found a way : )



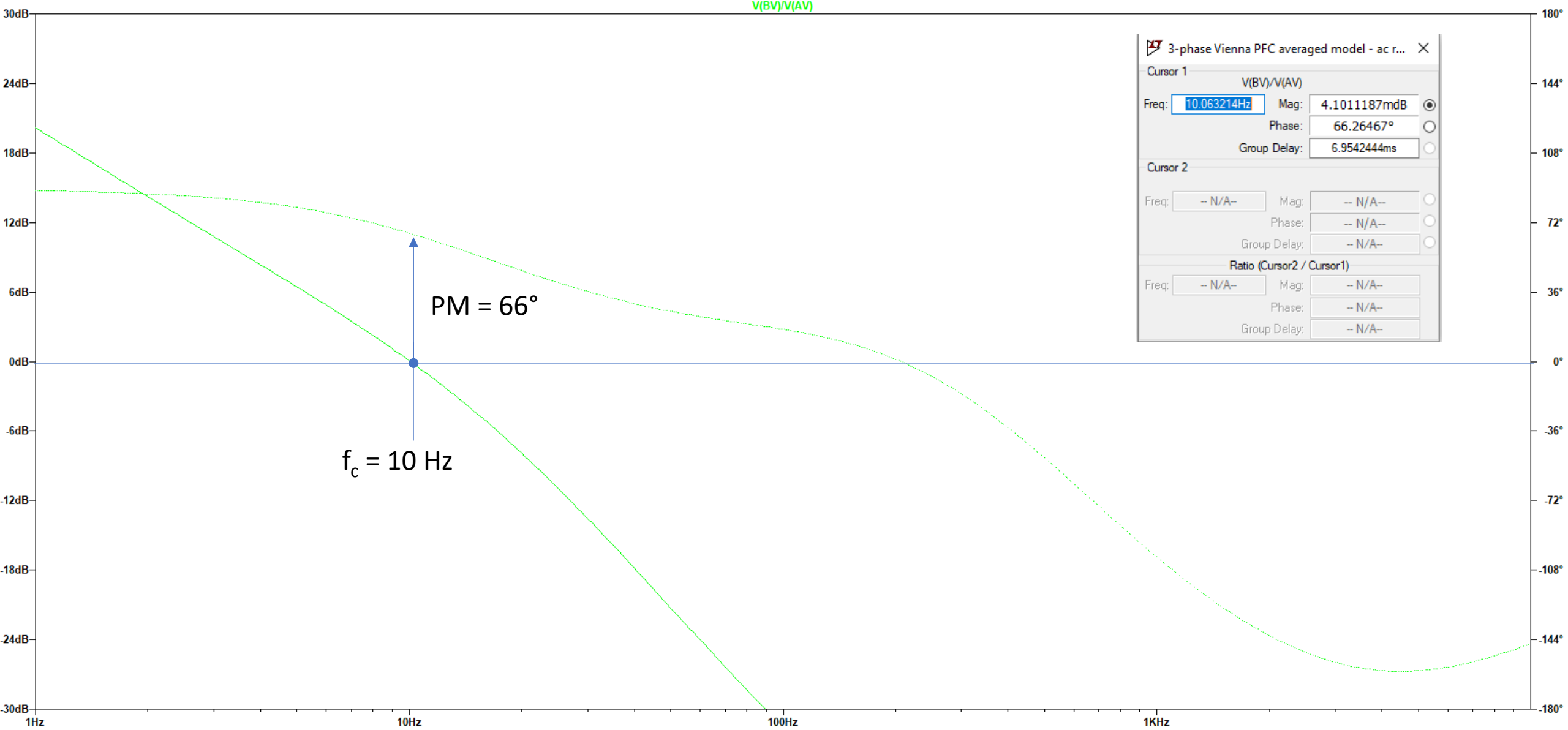
```
.ac dec 100 1 10k
.nodeset V(vout)=800 V(vo_2)=400
*
```

As I rarely give up, I've tried to keep one cap initialized (the low-side cap) to 400 V and added two .nodeset statements. It worked and the bias point is correct considering the given operating conditions. However, it is quite sensitive and might be an issue for a different setup. However, it validates the principle which is cool.

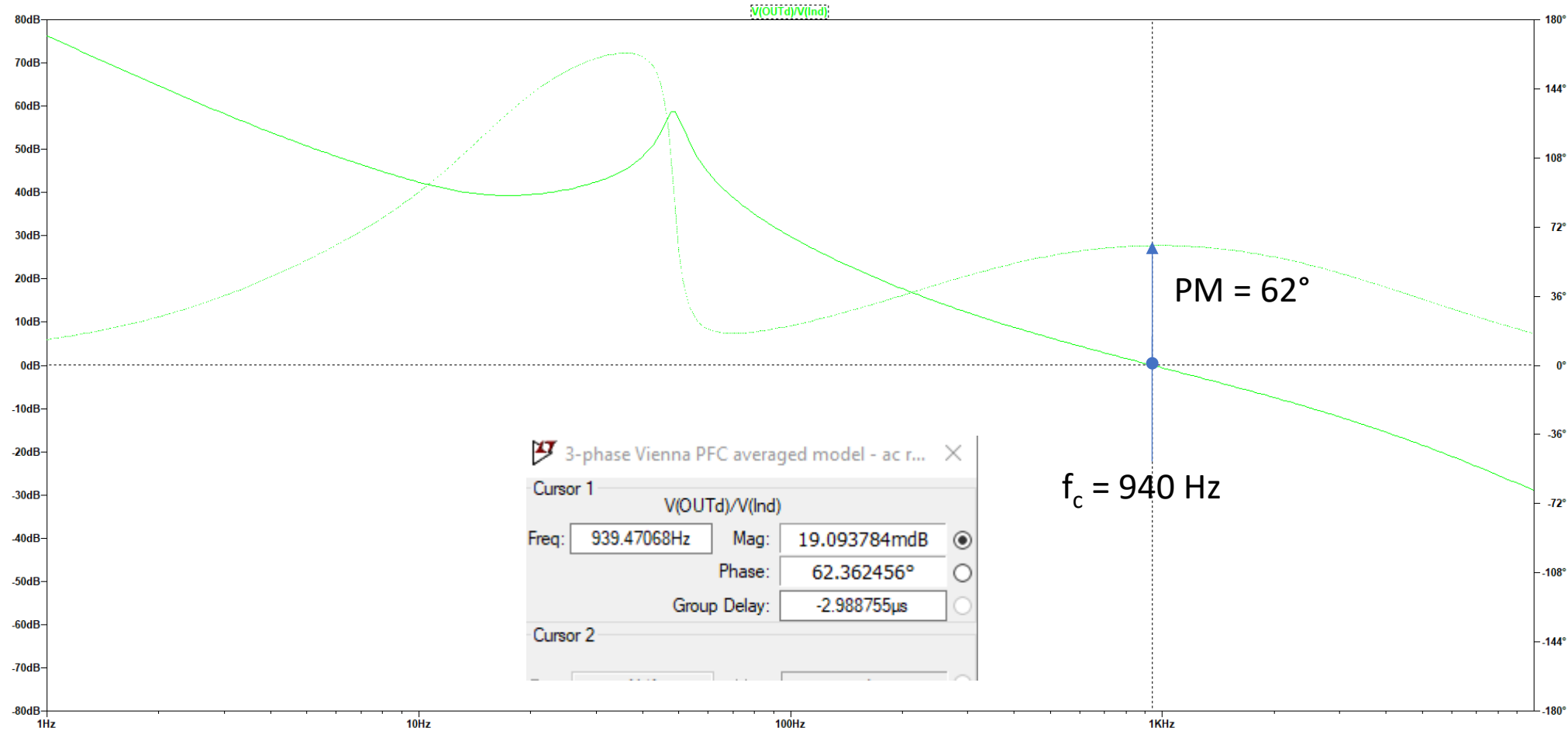


Plotting  $V(BV)/V(AV)$  gives the compensated loop gain. The control-to-output transfer function is obtained by plotting  $V(VOUT)/V(AV)$ .

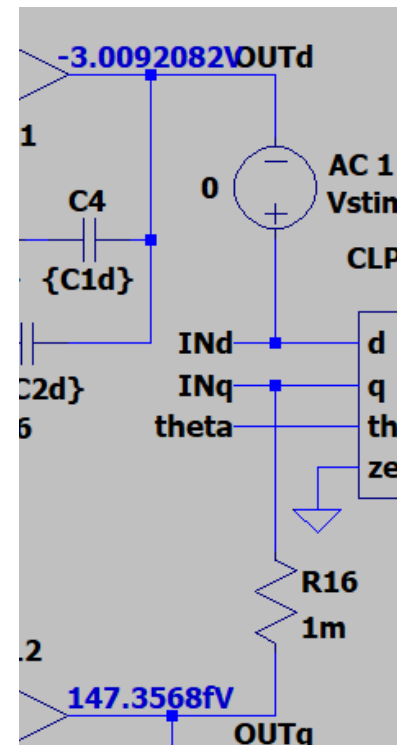
Type of sweep:	Decade
Number of points per decade:	100
Start frequency:	100m
Stop frequency:	100

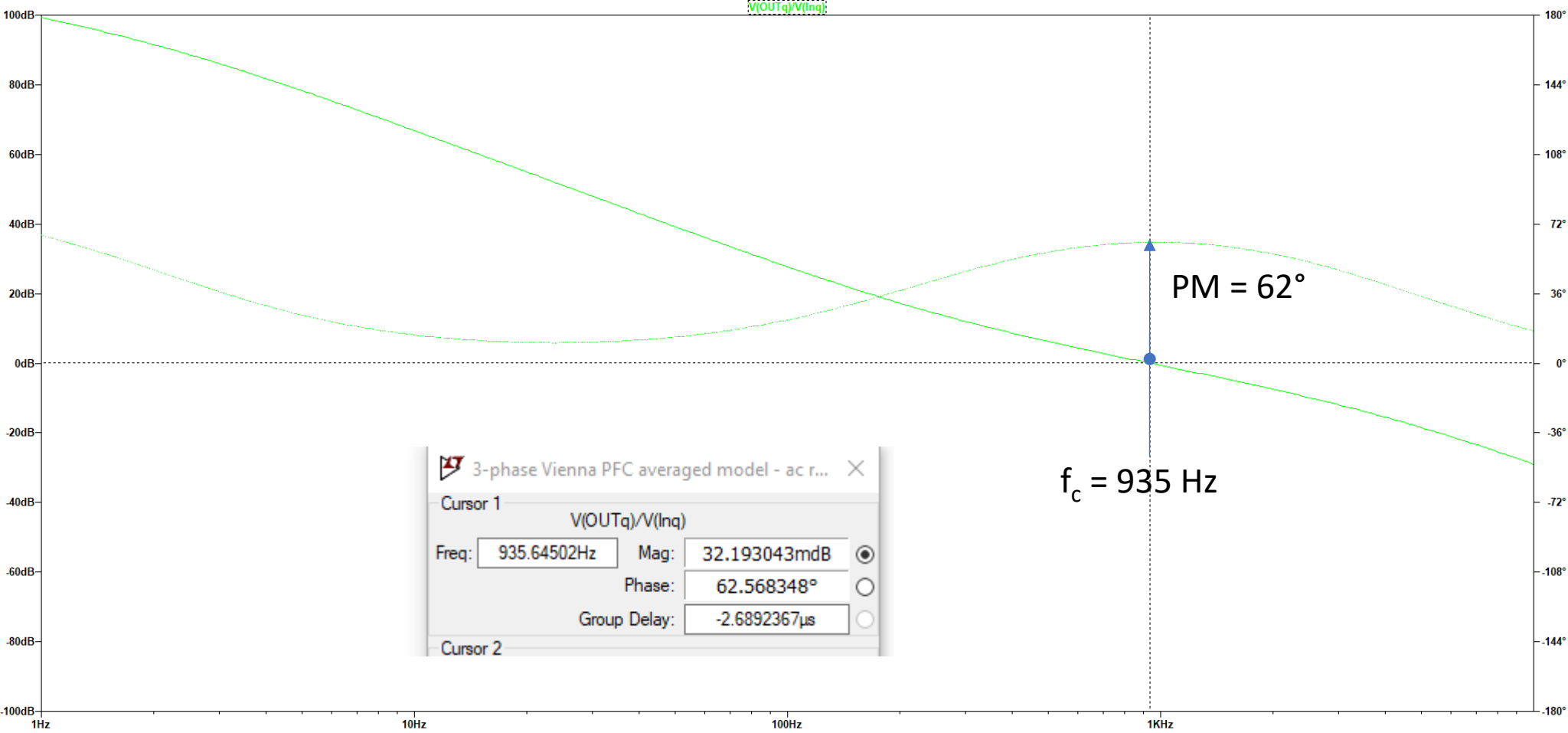


This is the compensated loop gain of the voltage loop.

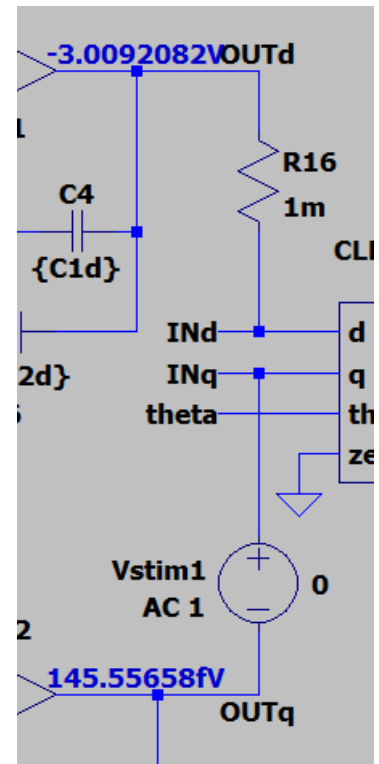


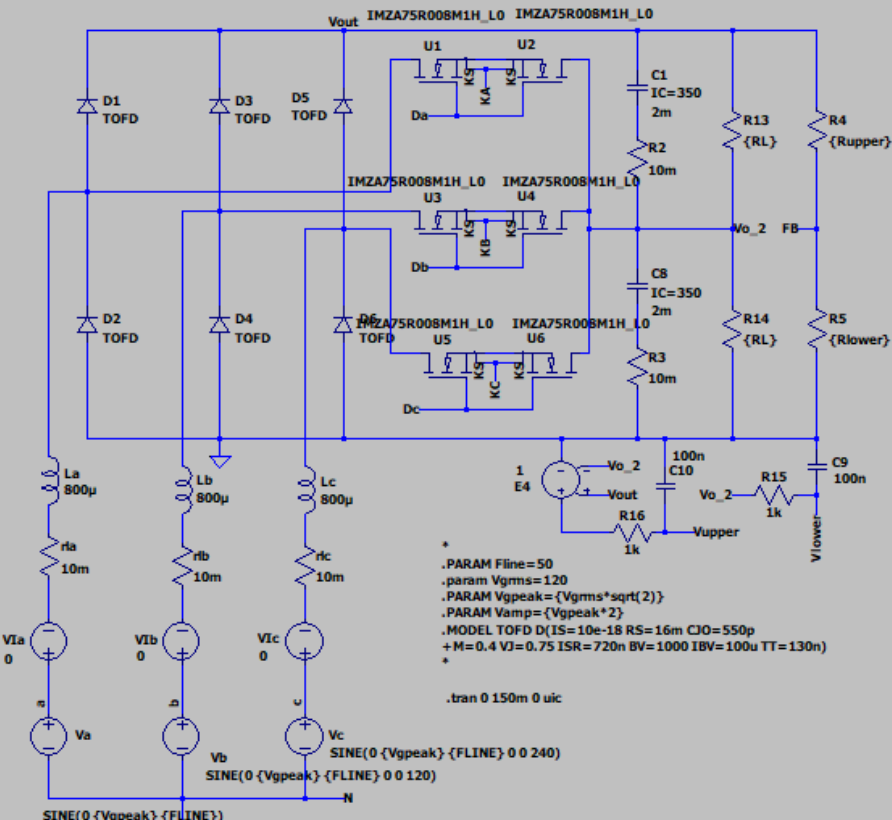
Now change the ac source to plot the d loop. Close the V-loop with  $R_{15}$  and plot  $V(OUTd)/V(Ind)$  for the compensated d-loop gain.





Now change the ac source to plot the q loop. Close the d-loop with  $R_{16}$  and plot  $V(OUTq)/V(INq)$  for the compensated q-loop gain.





```

.options abstol=1u vntol=1m reitoll=0.01 gmin=100p
+method=gear

.four 50 10 -1 I(Via)
.four 50 10 -1 I(Vib)
.four 50 10 -1 I(Vic)

.param GfcV=35 ; magnitude at crossover *
.param PSV=-62 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fcV=10 ; targeted crossover *
.param PMV=60 ; choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Rdd=100k
*
* Do not edit the below lines *
.param boostd={PMd-PSd-90}
.param Gd={10**(-Gfcd/20)}
.param kd={tan((boostd/2+45)*pi/180)}
.param fpd={fcd*kd}
.param fzd={fcd/kd}
.param C2d={1/(2*pi*fzd*Gd*kd*Rdd)}
.param C1d={C2d*(kd**2-1)}
.param R2d={kd/(C1d*2*pi*fcd)}
*
* Components for the q loop *
.param Gfcq=-1.2 ; magnitude at crossover *
.param PSq=-93 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fcq=1k ; targeted crossover *
.param PMq=60 ; choose phase margin at crossover *
*
.param Rdq=100k
*
* Do not edit the below lines *
.param boostq={PMq-PSq-90}
.param Gq={10**(-Gfcq/20)}
.param kq={tan((boostq/2+45)*pi/180)}
.param fpq={fcq*kq}
.param fzq={fcq/kq}
.param C2q={1/(2*pi*fpq*Gq*kq*Rdq)}
.param C1q={C2q*(kq**2-1)}
.param R2q={kq/(C1q*2*pi*fcq)}
*

.LIB IFX_CoolSiC_Gen1_Industrial_750V.lib

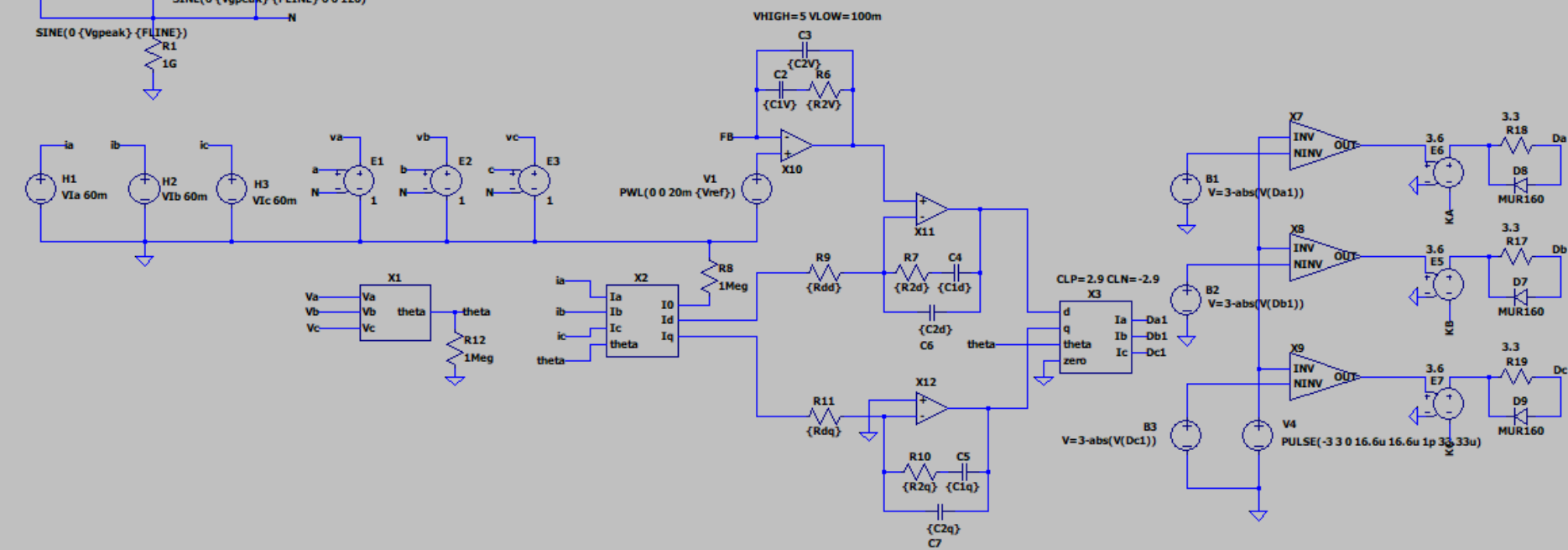
.model MUR160 D(IS=7.4f RS=50m CJO=17p
+M=0.50 vj=0.75 ISR=940p
+BV=600 ibv=100u tt=120n)

```

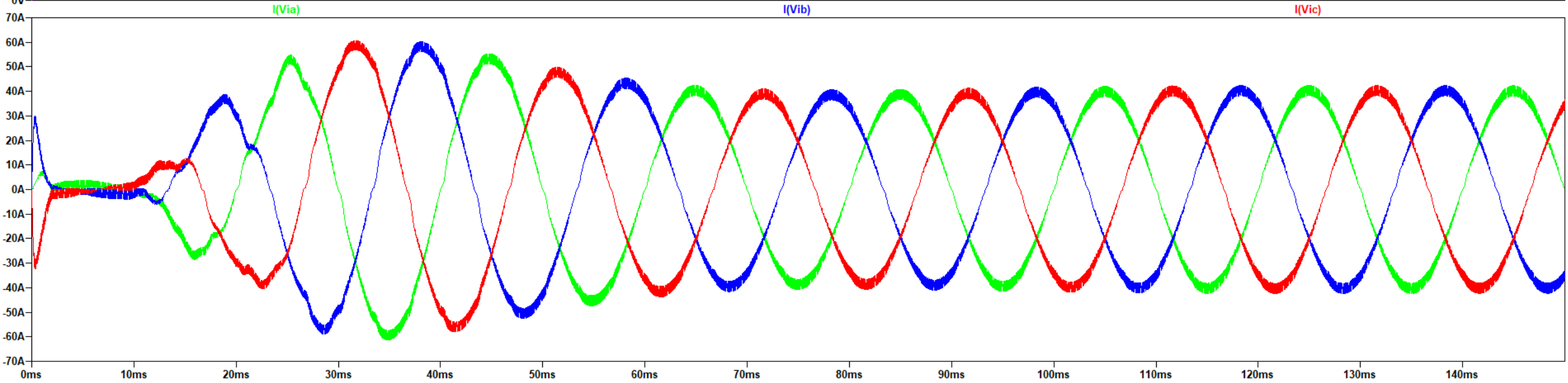
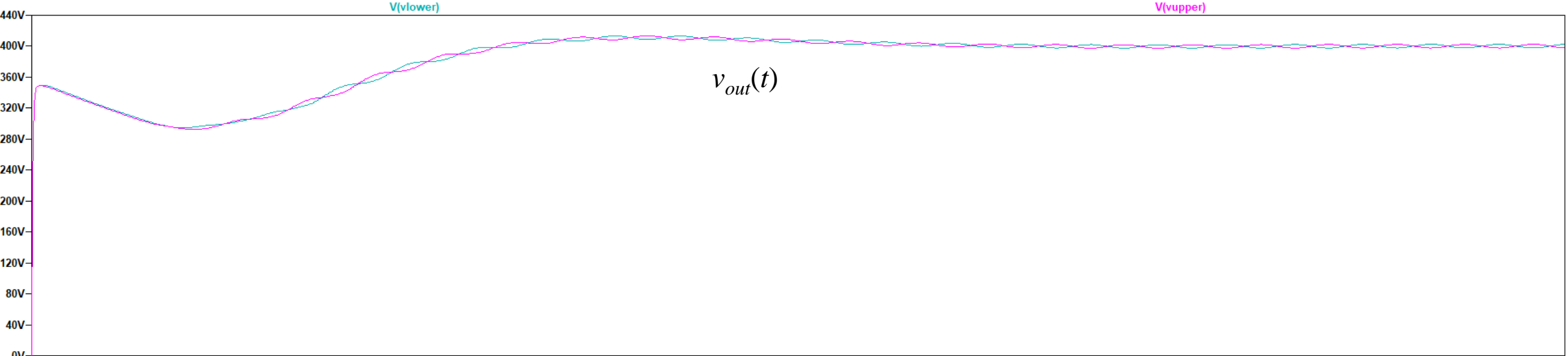
```

* Components for the d loop *
.param GfcV=-1.2 ; magnitude at crossover *
.param PSd=-93 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fcd=1k ; targeted crossover *
.param PMd=60 ; choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.param Rdd=100k
*
* Do not edit the below lines *
.param boostd={PMd-PSd-90}
.param Gd={10**(-Gfcd/20)}
.param kd={tan((boostd/2+45)*pi/180)}
.param fpd={fcd*kd}
.param fzd={fcd/kd}
.param C2d={1/(2*pi*fzd*Gd*kd*Rdd)}
.param C1d={C2d*(kd**2-1)}
.param R2d={kd/(C1d*2*pi*fcd)}
*
* Components for the q loop *
.param Gfcq=-1.2 ; magnitude at crossover *
.param PSq=-93 ; phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.param fcq=1k ; targeted crossover *
.param PMq=60 ; choose phase margin at crossover *
*
.param Rdq=100k
*
* Do not edit the below lines *
.param boostq={PMq-PSq-90}
.param Gq={10**(-Gfcq/20)}
.param kq={tan((boostq/2+45)*pi/180)}
.param fpq={fcq*kq}
.param fzq={fcq/kq}
.param C2q={1/(2*pi*fpq*Gq*kq*Rdq)}
.param C1q={C2q*(kq**2-1)}
.param R2q={kq/(C1q*2*pi*fcq)}
*

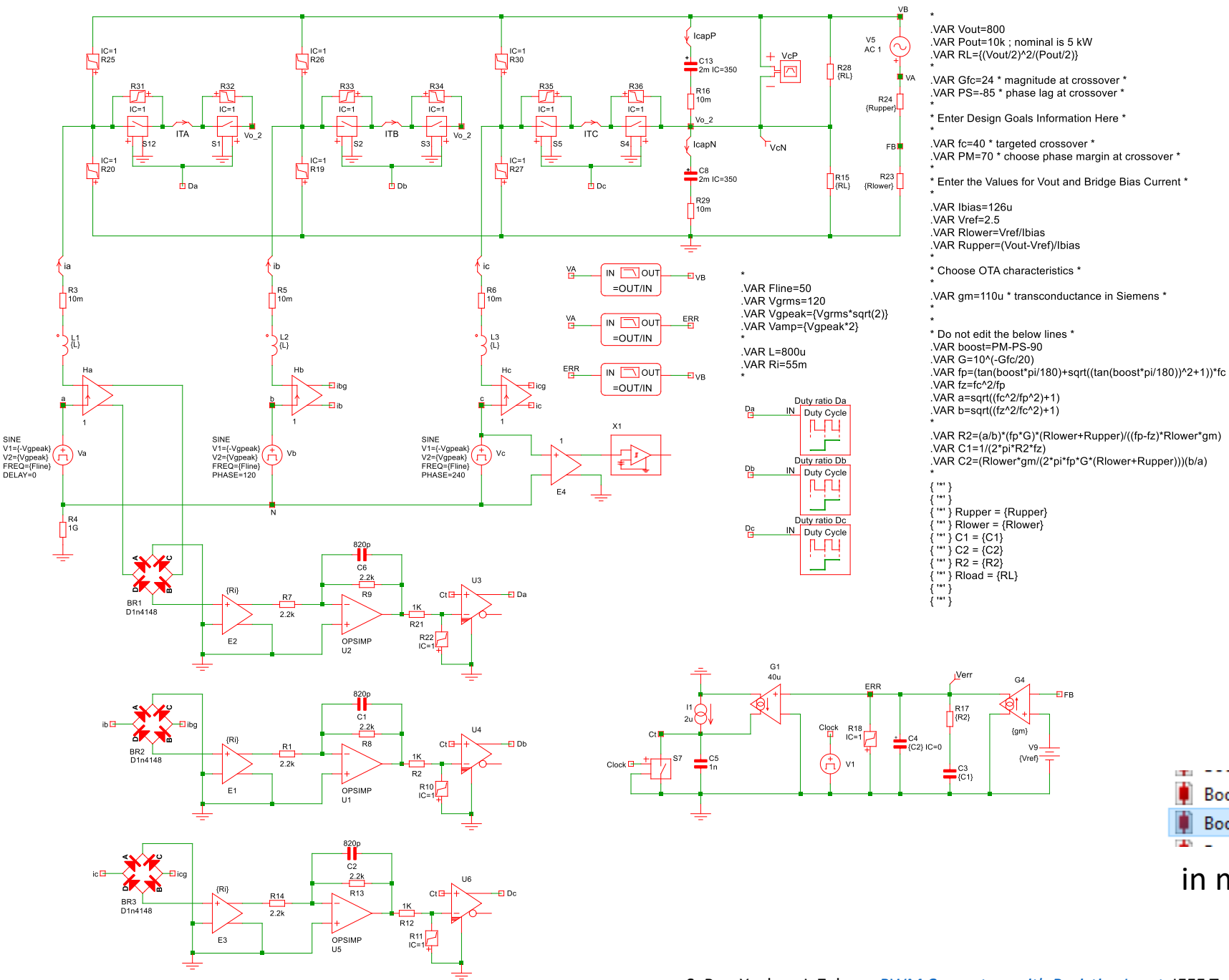
```



The perfect switches have been replaced by SiC transistors models to check if the rectifier still works well in this mode.



$V_{in} = 120 \text{ V rms}, P_{out} = 10 \text{ kW}$



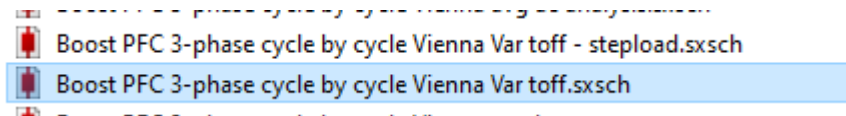
```

*
.VAR Vout=800
.VAR Pout=10k ; nominal is 5 kW
.VAR RL={(Vout/2)^2/(Pout/2)}
*
.VAR Gfc=24 * magnitude at crossover *
.VAR PS=-85 * phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.VAR fC=40 * targeted crossover *
.VAR PM=70 * choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.VAR Ibias=126u
.VAR Vref=2.5
.VAR Rlower=Vref/Ibias
.VAR Rupper=(Vout-Vref)/Ibias
*
* Choose OTA characteristics *
*
.VAR gm=110u * transconductance in Siemens *
*
* Do not edit the below lines *
.VAR boost=PM-PS-90
.VAR G=10^(-Gfc/20)
.VAR fp=(tan(boost*pi/180)+sqrt((tan(boost*pi/180))^2+1))*fc
.VAR fz=fc^2/fp
.VAR a=sqrt((fz^2/fc^2)+1)
.VAR b=sqrt((fz^2/fc^2)+1)
*
.VAR R2=(a/b)*(fp*G)*(Rlower+Rupper)/((fp-fz)*Rlower*gm)
.VAR C1=1/(2*pi*R2*fz)
.VAR C2=(Rlower*gm/(2*pi*fp*G*(Rlower+Rupper)))/(b/a)
*
{**}
{**}
{**} Rupper = {Rupper}
{**} Rlower = {Rlower}
{**} C1 = {C1}
{**} C2 = {C2}
{**} R2 = {R2}
{**} Rload = {RL}
{**}

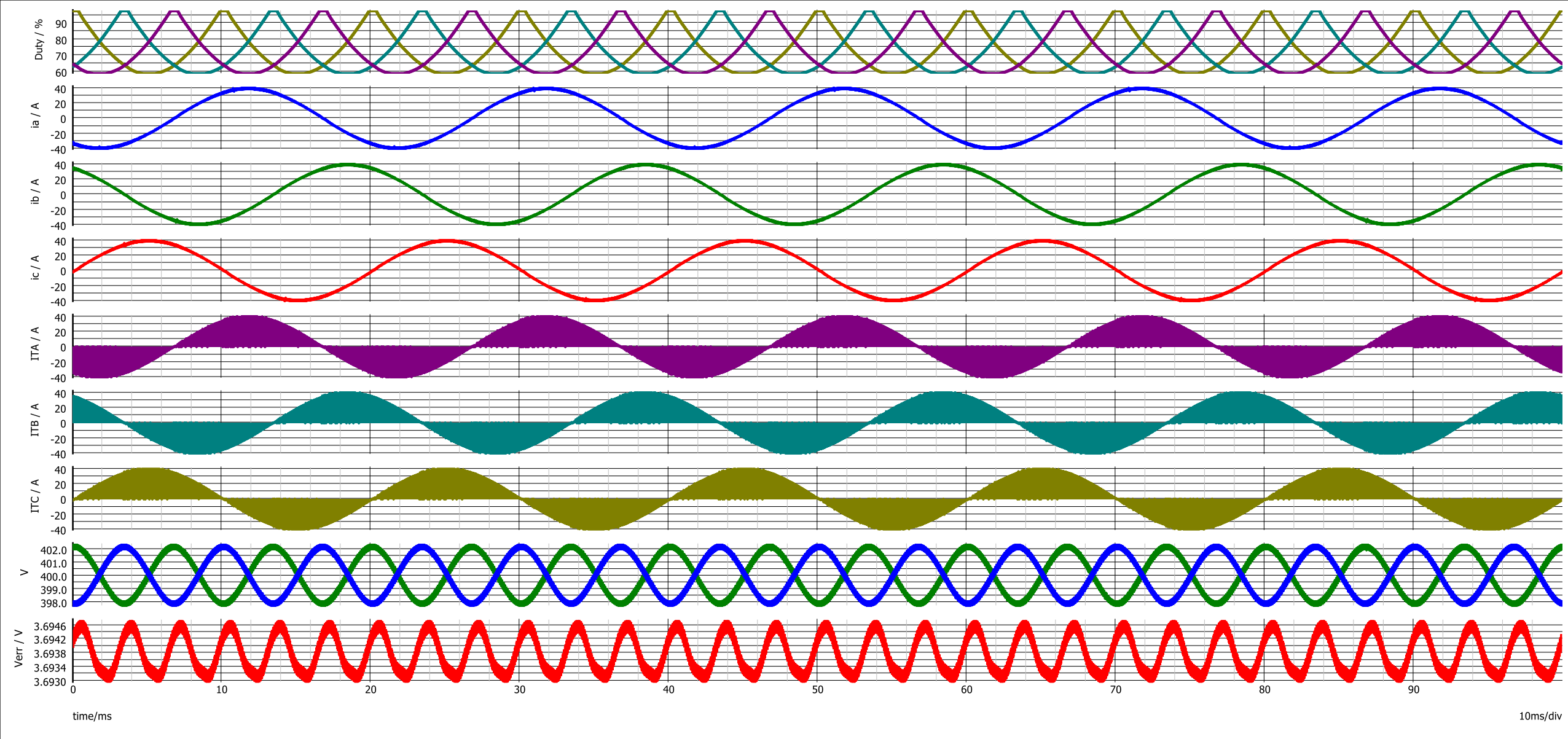
```

This is another simplified way to control the 3-phase Vienna rectifier. I am using the method documented by Sam Ben-Yaakov in the paper referenced below. I have adapted it to this 3-phase rectifier and it brings excellent results without sensing the high-voltage rail.

The good thing is that it runs on SIMPLIS and I can extract the small-signal response of the voltage loop via a POP and set a crossover frequency of 40 Hz with a good phase margin.

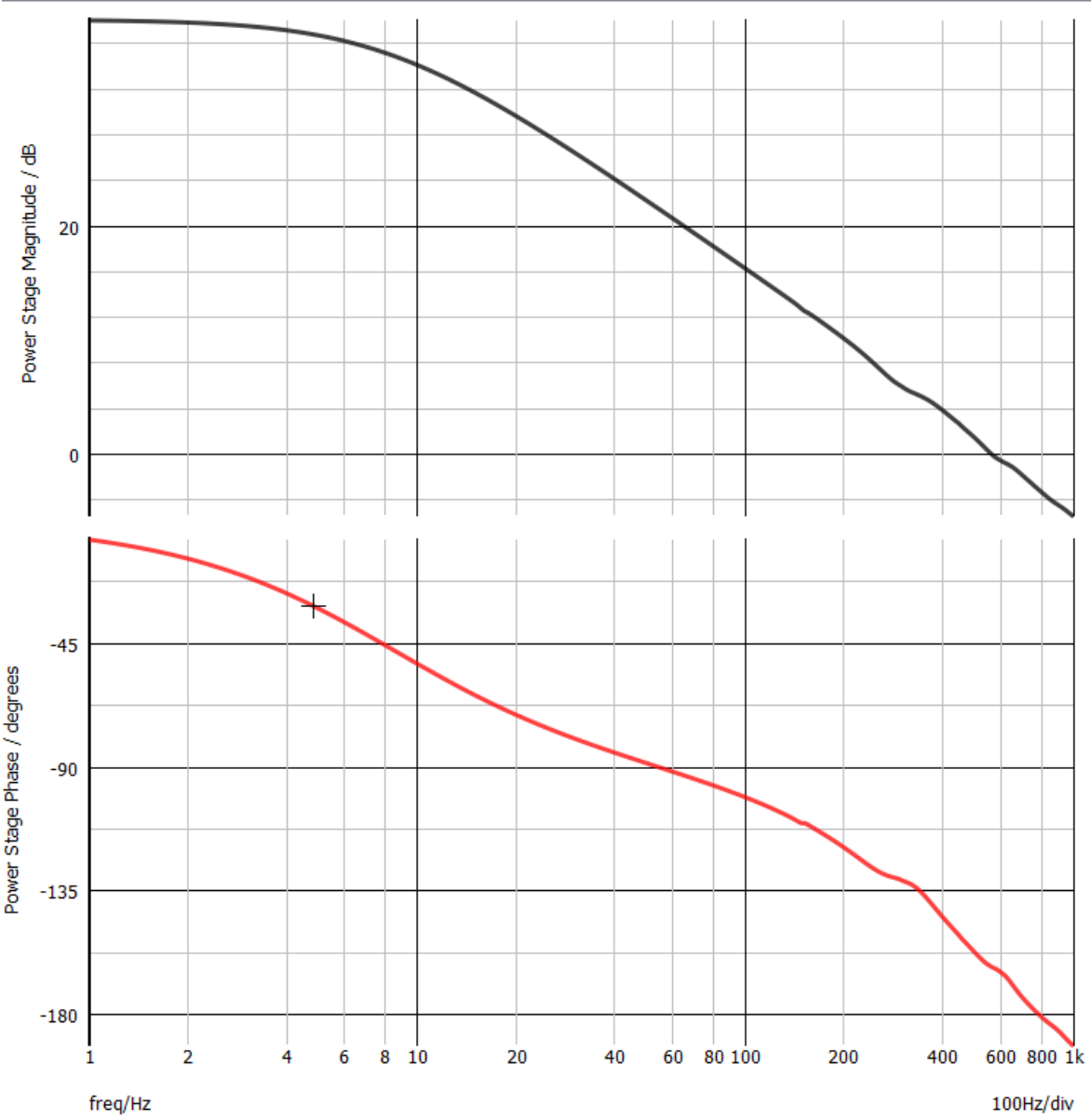


in my [ZIP](#) file.

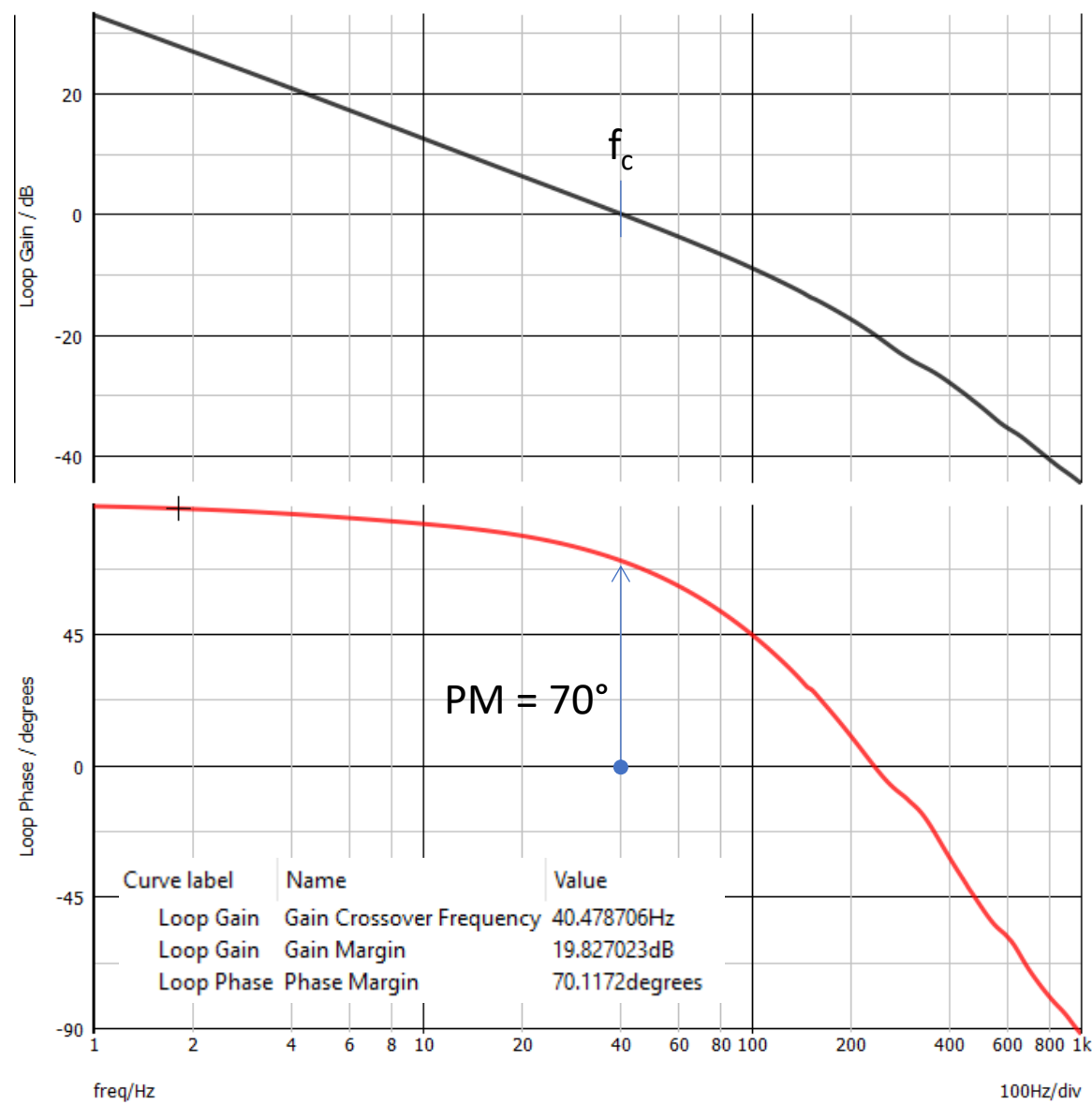


Curve label	Name	Value
ia	Distortion/cycle	3.23318%
ib	Distortion/cycle	3.23793%
ic	Distortion/cycle	3.23321%

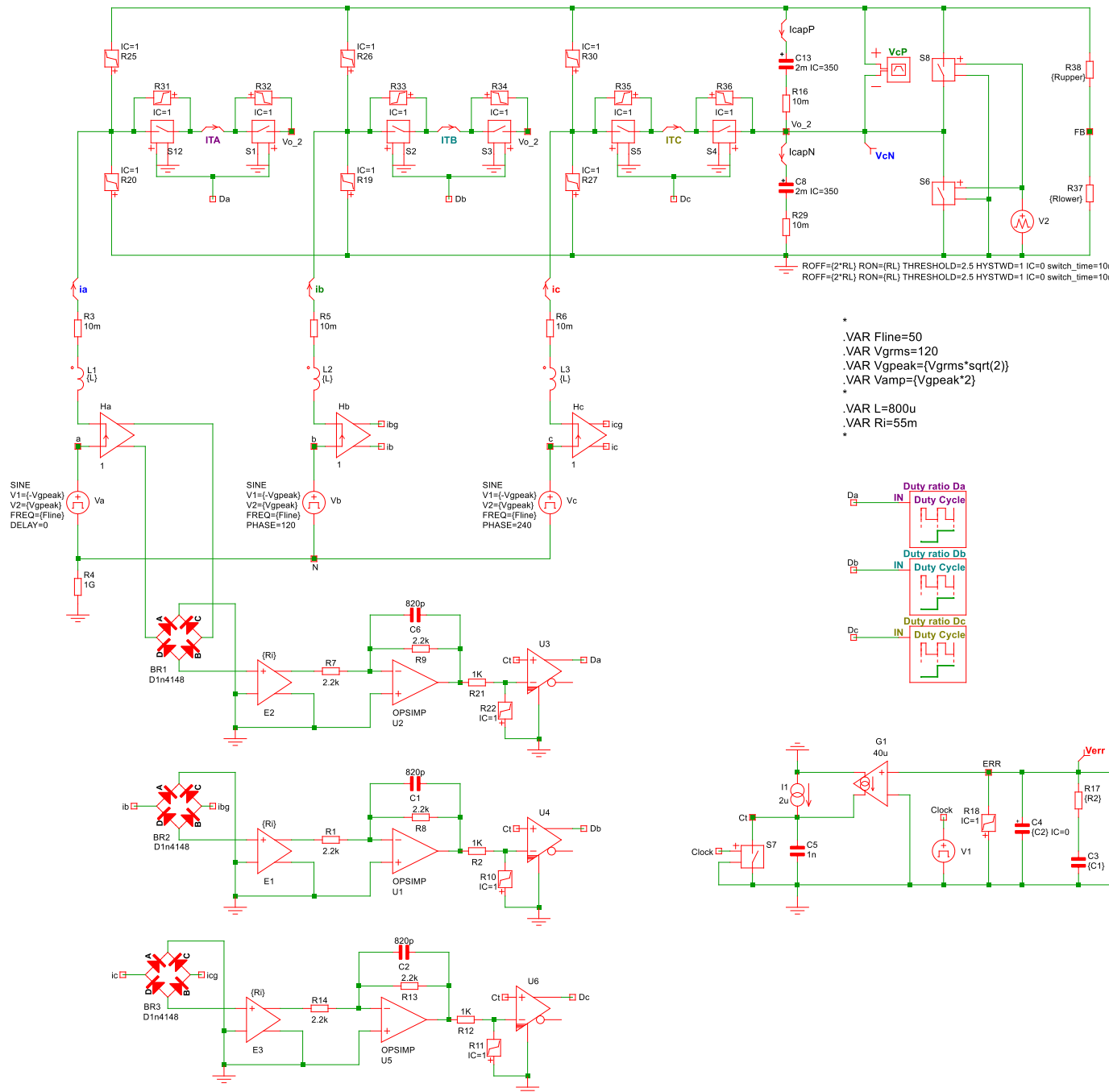
$V_{in} = 120 \text{ V rms}, P_{out} = 10 \text{ kW}$



Power stage response



Compensated loop gain

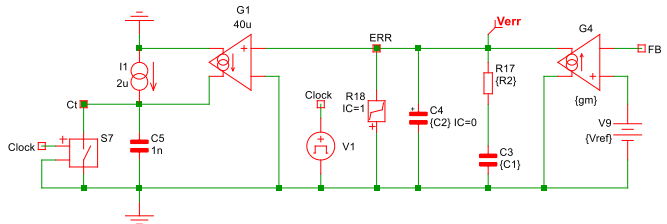


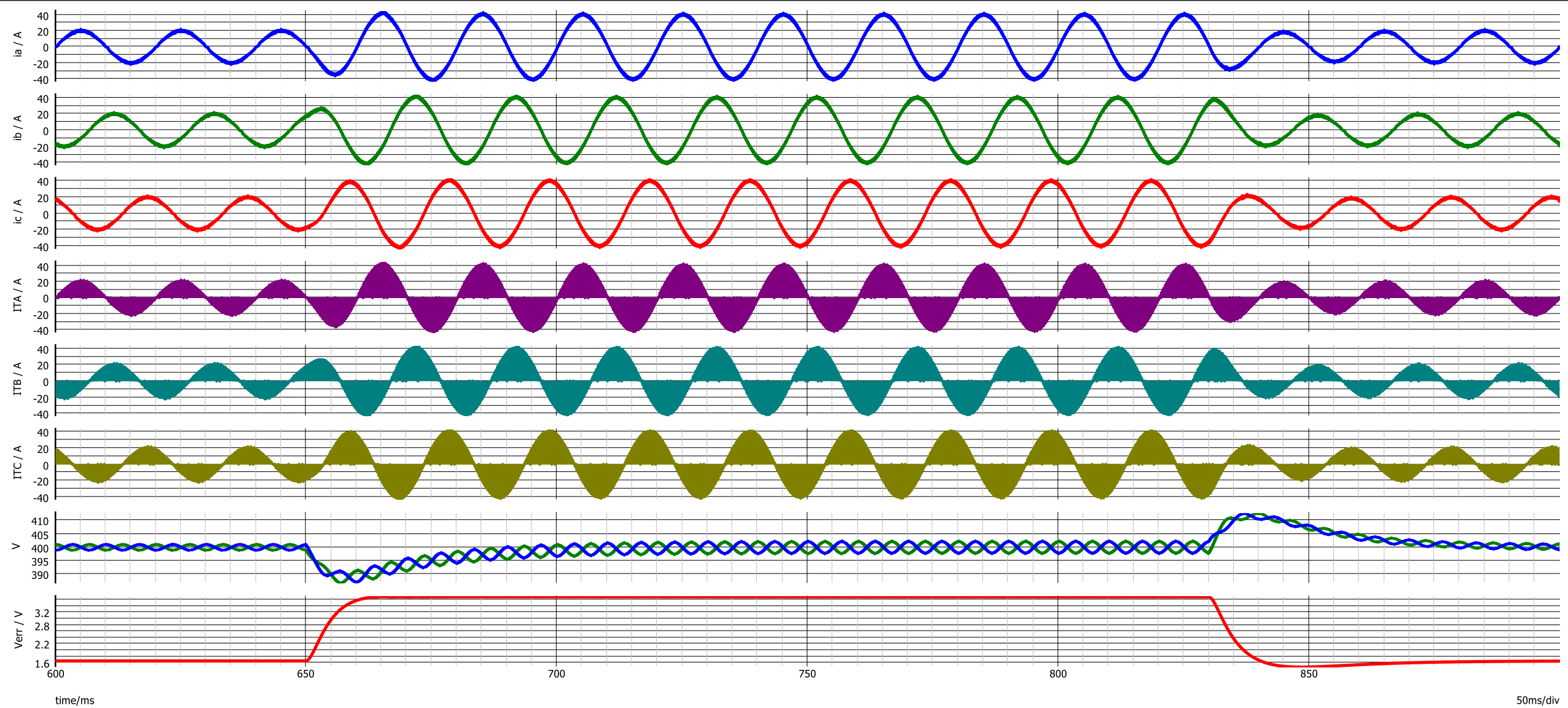
```

*
.VAR Vout=800
.VAR Pout=10k ; nominal is 5 kW
.VAR RL=((Vout/2)^2/(Pout/2))
*
.VAR Gfc=24 * magnitude at crossover *
.VAR PS=-85 * phase lag at crossover *
*
* Enter Design Goals Information Here *
*
.VAR fc=40 * targeted crossover *
.VAR PM=70 * choose phase margin at crossover *
*
* Enter the Values for Vout and Bridge Bias Current *
*
.VAR Ibias=126u
.VAR Vref=2.5
.VAR Rlower=Vref/Ibias
.VAR Rupper=(Vout-Vref)/Ibias
*
* Choose OTA characteristics *
*
.VAR gm=110u * transconductance in Siemens *
*
* Do not edit the below lines *
.VAR boost=PM-PS-90
.VAR G=10^(Gfc/20)
.VAR fp=(tan(boost*pi/180)+sqrt((tan(boost*pi/180))^2+1))*fc
.VAR fz=fc^2/fp
.VAR a=sqrt((fc^2/fp^2)+1)
.VAR b=sqrt((fz^2/fc^2)+1)
*
.VAR R2=(a/b)*(fp*G)*(Rlower+Rupper)/((fp-fz)*Rlower*gm)
.VAR C1=1/(2*pi*R2*fz)
.VAR C2=(Rlower*gm/(2*pi*fp*G*(Rlower+Rupper)))/(b/a)
*
{ "" }
{ "" }
{ "" } Rupper = {Rupper}
{ "" } Rlower = {Rlower}
{ "" } C1 = {C1}
{ "" } C2 = {C2}
{ "" } R2 = {R2}
{ "" } Rload = {RL}
{ "" }
{ "" }

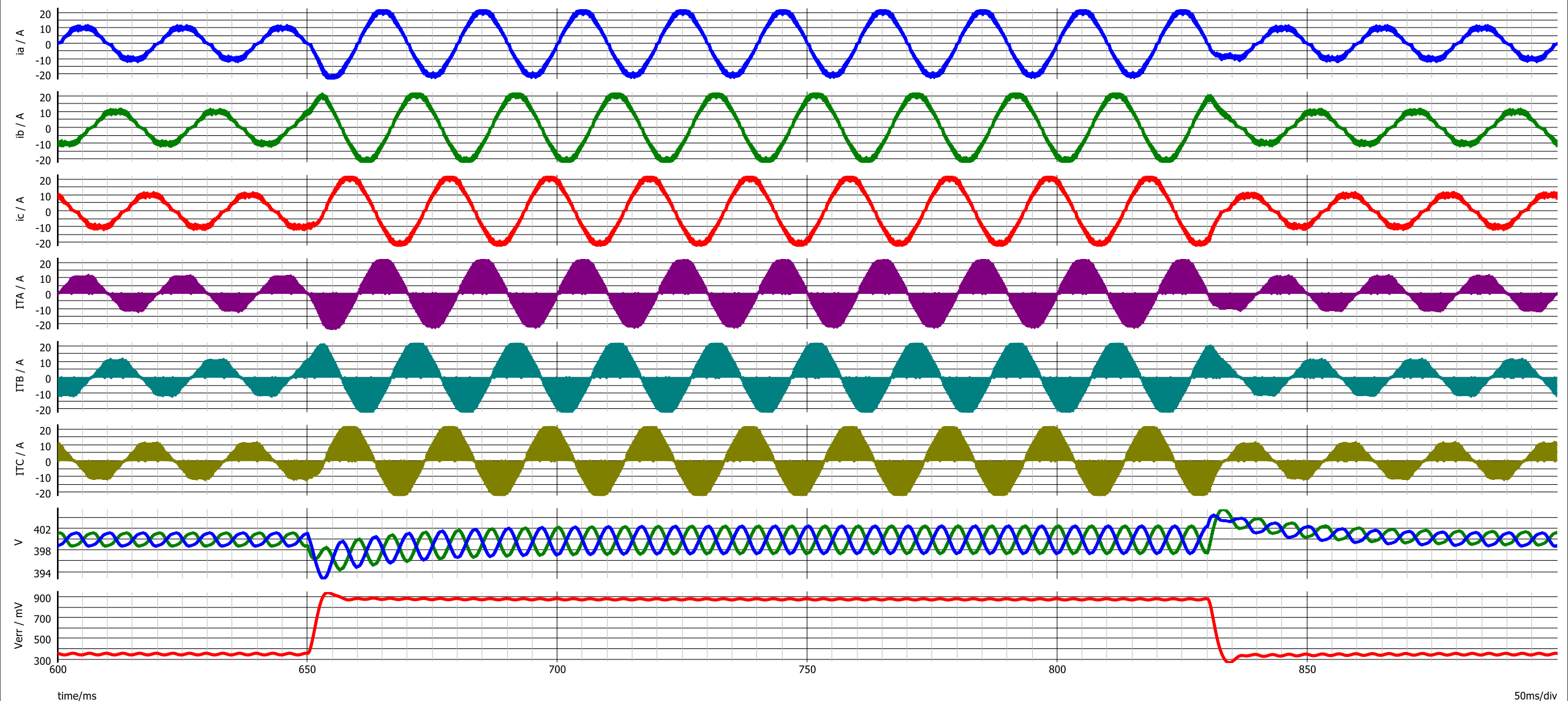
```

The final test includes the transient load step.

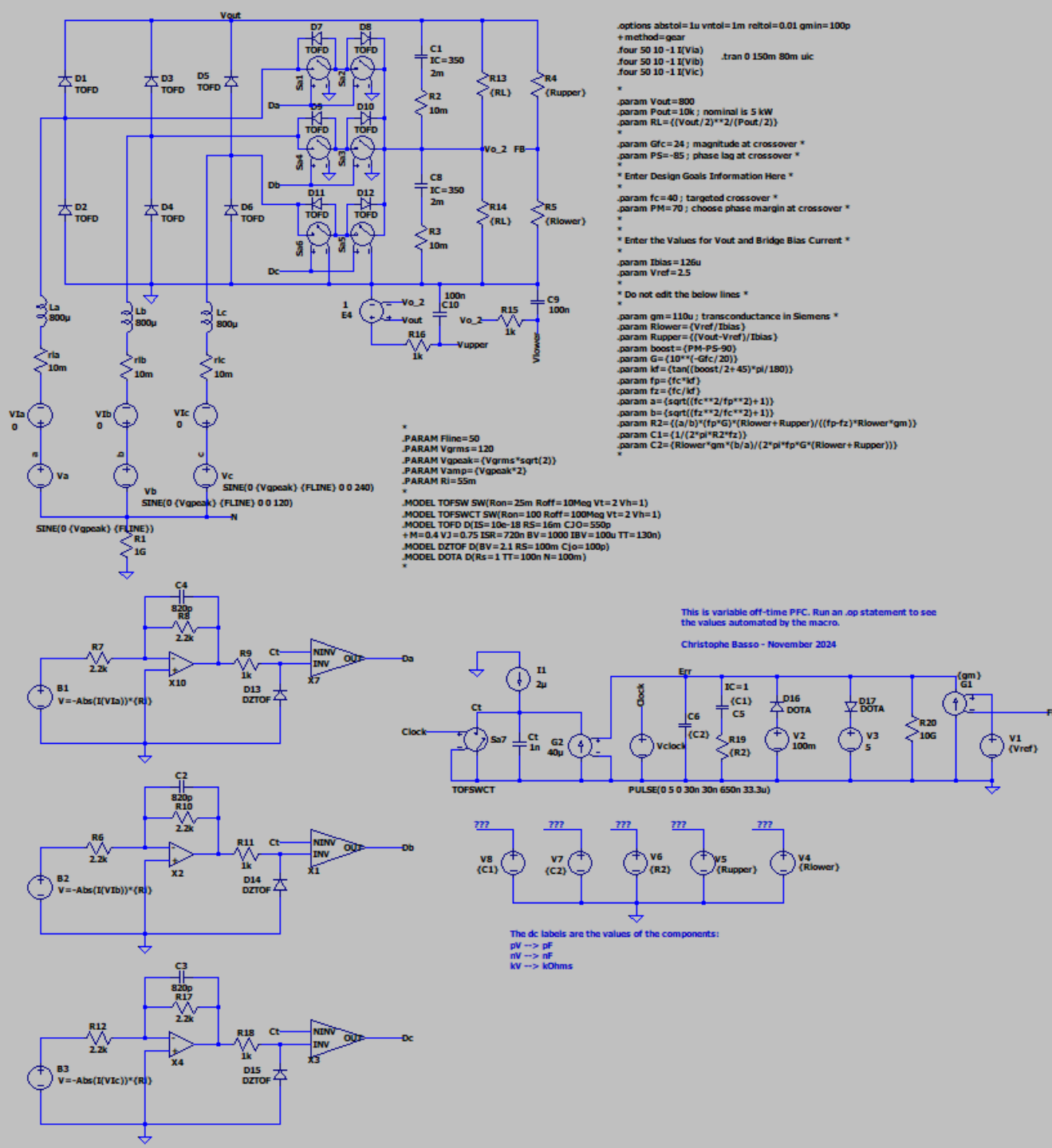




$V_{in} = 120 \text{ V rms}$ ,  $P_{out}$  stepped from 5 to 10 kW

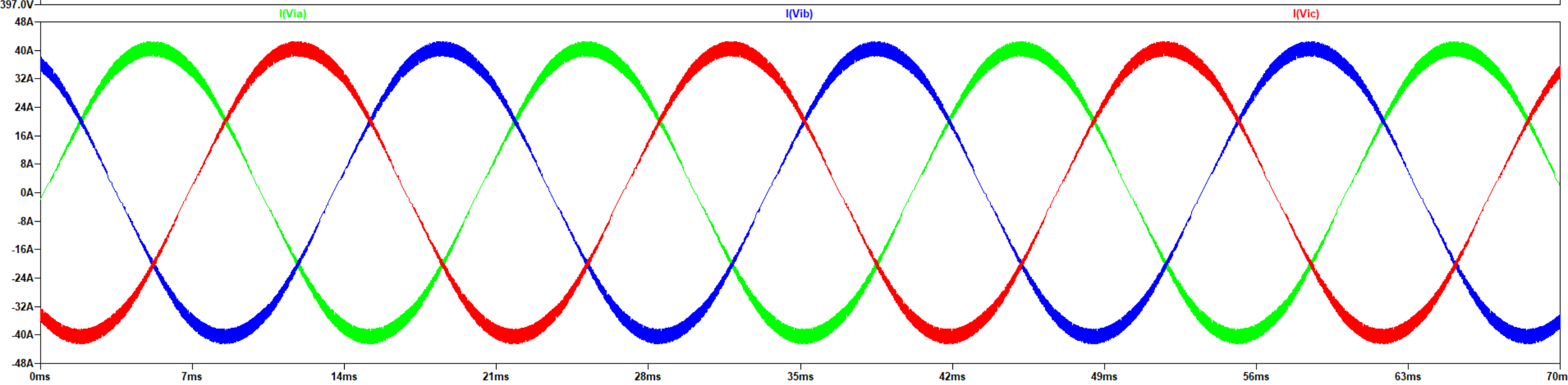
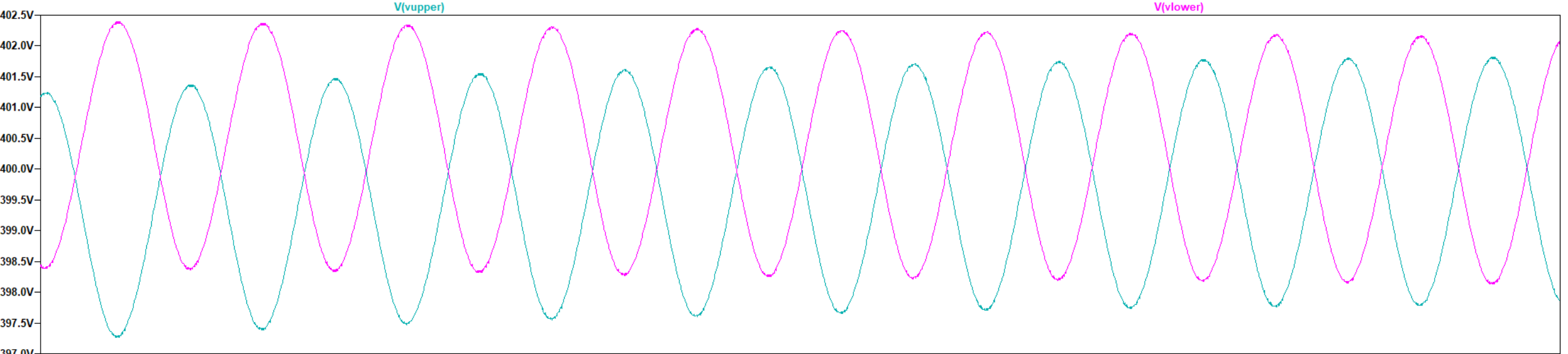


$V_{in} = 230$  V rms,  $P_{out}$  stepped from 5 to 10 kW



This is the LTspice version of the variable off-time 3-phase VIENNA rectifier and it simulates fast. The rectifier used in SIMPLIS is no longer necessary and I used an ABS in-line equation to rectify the input currents for phases a, b and c.

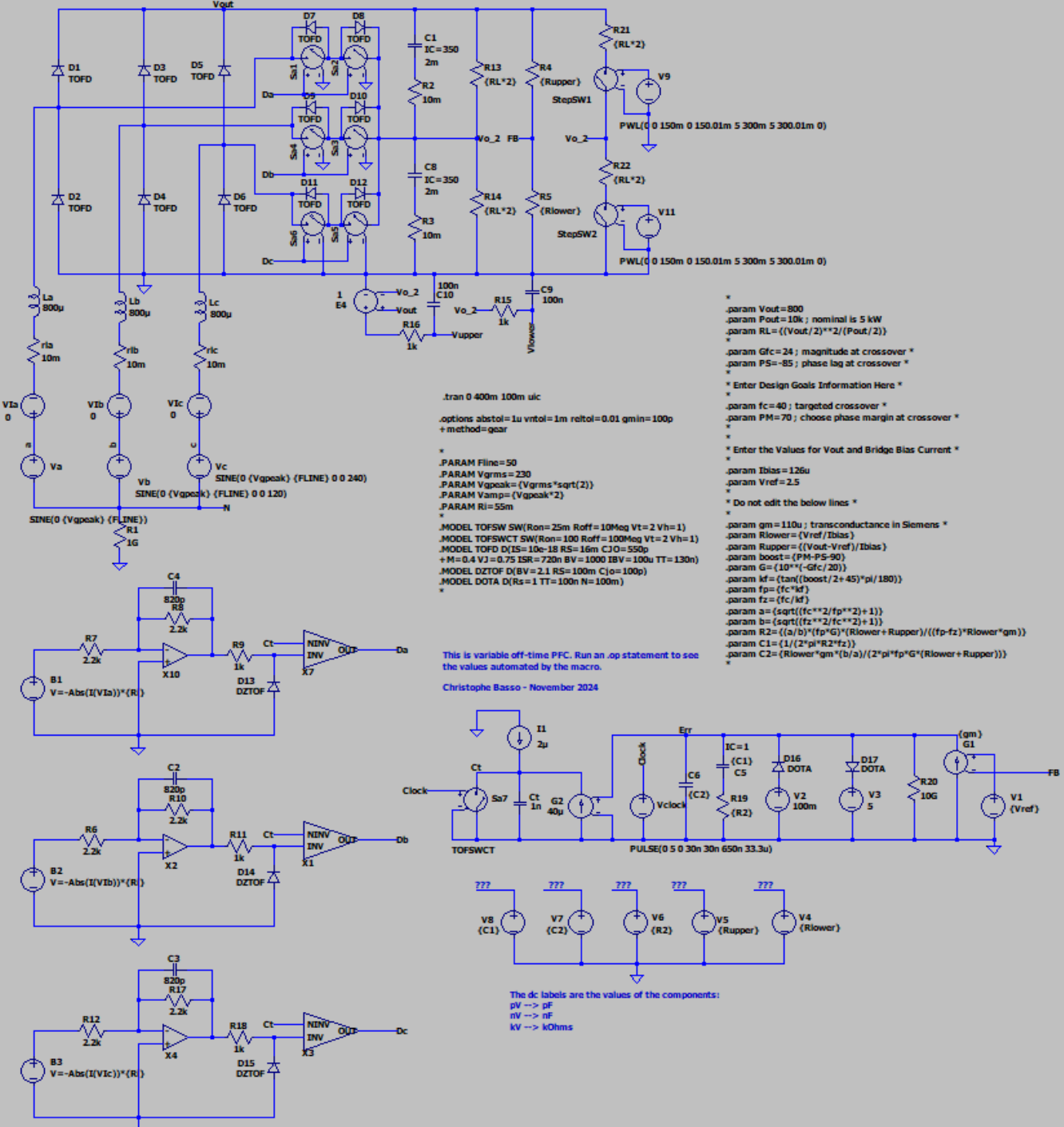
The right-side macro automates the type 2 OTA compensator for a 10-Hz crossover frequency as obtained in SIMPLIS. Running an .op analysis will display the components values as bias points in the schematic diagram.

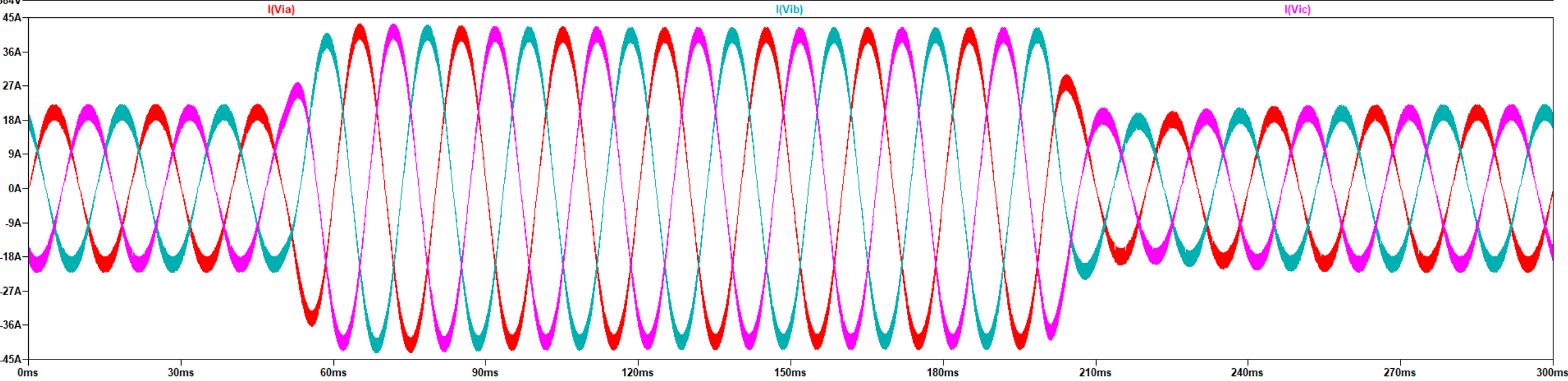
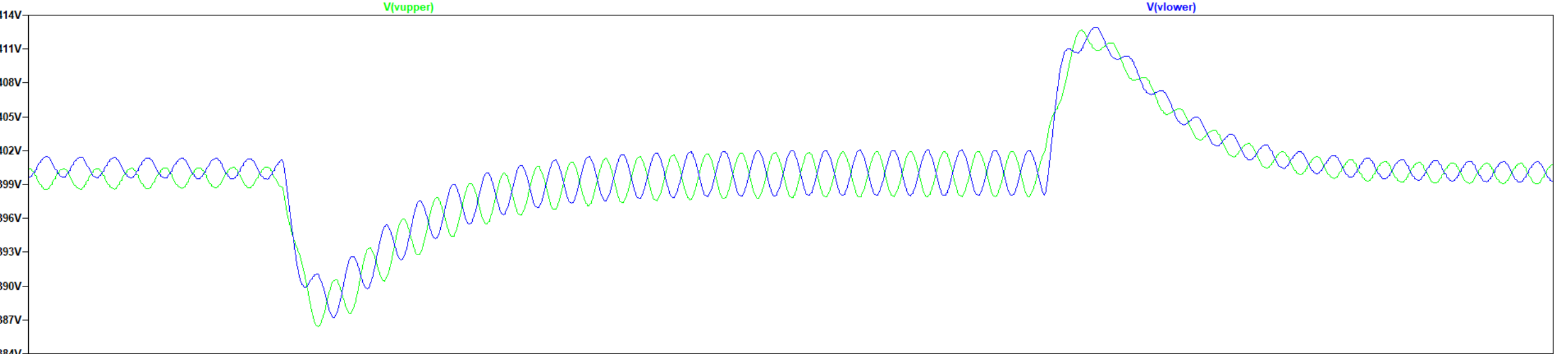


$V_{in} = 120 \text{ V rms}$ ,  $P_{out} = 10 \text{ kW}$

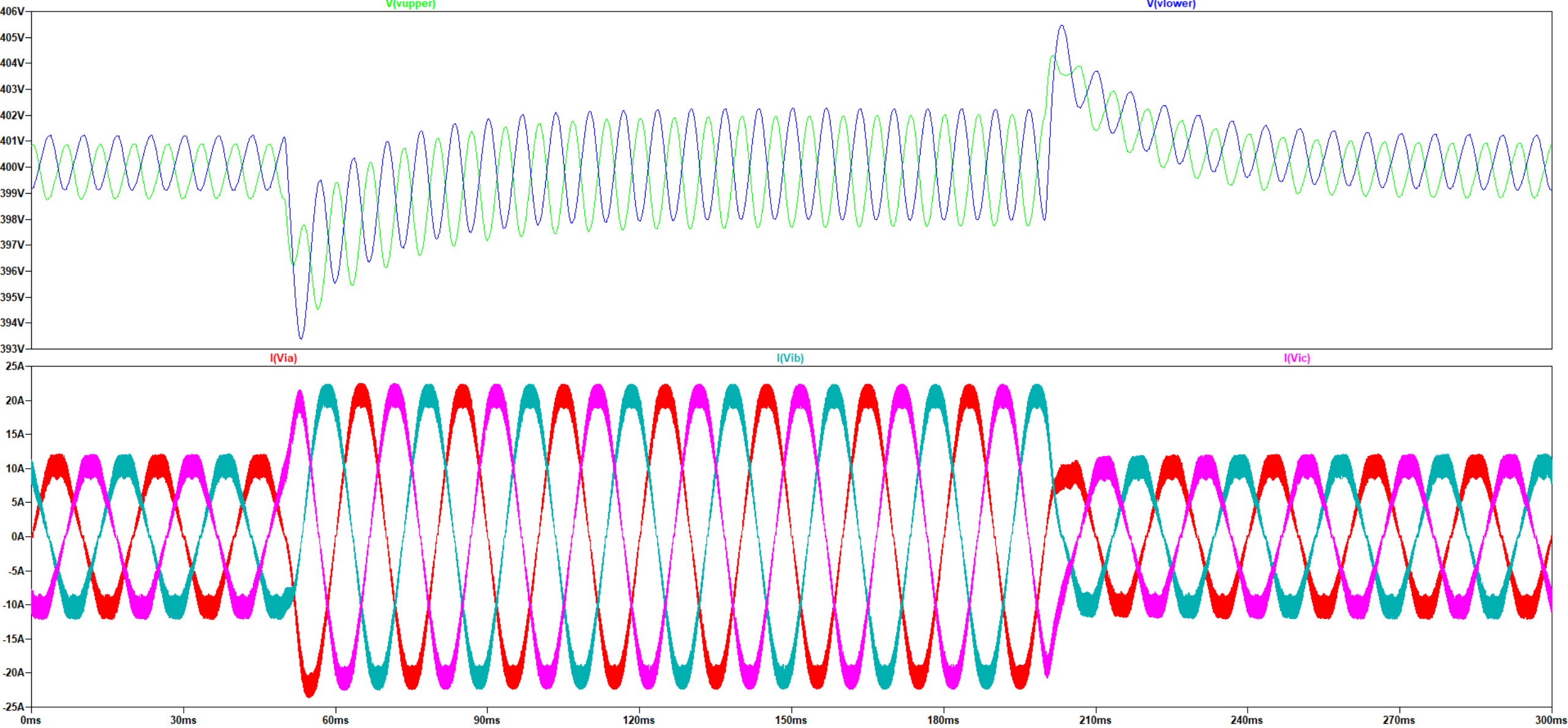
Total Harmonic Distortion: 3.232831%

This is the same circuit now equipped with two controlled switches on the output, toggling the load from 50 to 100% of its nominal value (5 kW to 10 kW).





$V_{in} = 120 \text{ V rms}$ ,  $P_{out}$  stepped from 5 to 10 kW



$V_{in} = 230 \text{ V rms}$ ,  $P_{out}$  stepped from 5 to 10 kW