The Flyback Converter with Leakage Inductance
Part I – Hardware Description

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The flyback converter frequency response operated in voltage-mode control (VM) and driven in Continuous Conduction Mode (CCM) is that of a second-order system. If the vast majority of analyses predict a transfer function whose quality factor is solely affected by the various losses (ohmic paths, magnetic losses, recovery time-related losses and so on), very few tackle the damping effect brought by the leakage inductance. However, transient simulations predict the damping of output oscillations as the leakage inductance increases. Because formulas available in the literature do not reflect this effect, a new model is necessary and will be described in the present paper.

The Flyback Converter in CCM

A perfect CCM flyback converter transmits power in two operating cycles: 1) the on-time t_{on} during which the primary-side power switch *SW* closes and energy builds up in the transformer primary inductance L_p 2) during the off-time t_{off} where the switch opens and energy is transferred to the secondary side via diode *D*. However, when scrutinizing the waveforms in a prototype, one can distinguished more states than the basic explanation describes. **Figure 1** shows a typical converter featuring a transformer affected by a leakage inductance l_{leak}. When the power switch closes, the input voltage is applied across the transformer primary inductance L_p, neglecting the switch ohmic losses. Looking closer to the schematic, this is not exactly V_{in} that is applied since a divider made of L_p and l_{leak} is at play here. The voltage across L_p during that moment is thus

$$V_{L_p}\Big|_{t_{on}} = V_{in}\frac{L_p}{L_p + l_{leak}} \tag{1}$$

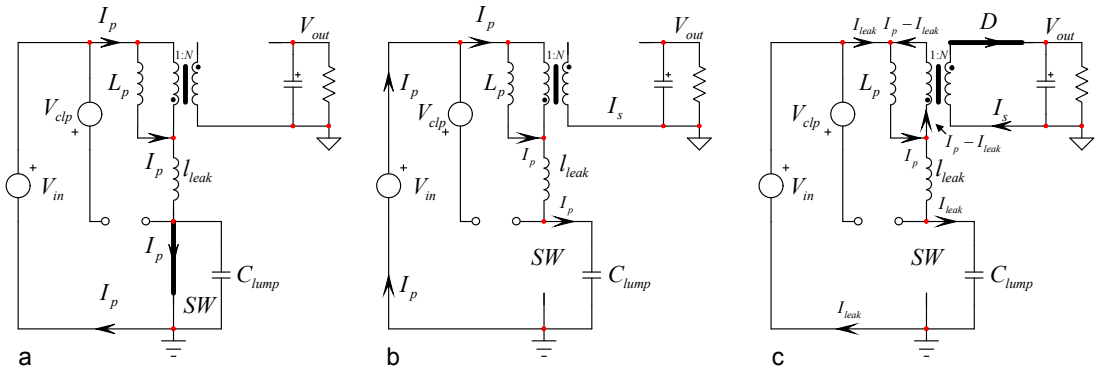

Figure 1: The operating states of a flyback converter show energy storage in the primary side followed by energy circulation in the secondary side when the power switch opens.

During t_{on} and considering the coupling dots, the secondary-side diode is blocked. As both L_p and l_{leak} appear in series, the current $i_p(t)$ circulating in these elements increases with a slope equal to

$$S_{on} = \frac{V_{in}}{L_p + l_{leak}} \tag{2}$$

When the controller instructs the switch to open, we jump to sketch (b). At this moment, the inductive current finds a path in the capacitance lumped at the drain node. This parasitic term is made of the MOSFET own non-linear capacitances seen from its drain terminal, C_{rss} and C_{oss} plus the various capacitances brought by the clamp diode, the transformer inter-windings capacitances and the output diode capacitance reflected to the primary. All these elements lump into a ground-referenced capacitor designated

as C_{lump}. As current flows in C_{lump}, the drain-source voltage quickly increases. The slope is not constant given the MOSFET non-linear capacitance. We can however say that the approximate slope of this voltage is given by

$$S_{drain} \approx \frac{I_{peak}}{C_{lump}} \tag{3}$$

In which I_{peak} is the current value when the switch opens. The drain voltage increases until the voltage across L_p reverses. At this moment, **Figure 1c**, the secondary diode becomes biased but no current circulates in the secondary yet. As both L_p and l_{leak} are energized, l_{leak} forces a current into the lump capacitance which continues its charge. Because of the series connection, the current in L_p and l_{leak} are equal and the net current flowing in the secondary diode is 0. The drain voltage at which D begins its conduction is equal to

$$V_{DS} \approx V_{in} + \frac{V_{out} + V_f}{N} \tag{4}$$

The output voltage now flies back across L_p – hence the term *flyback* converter – and forces a downslope equal to

$$S_{off} = -\frac{V_{out} + V_f}{NL_p} \tag{5}$$

The drain node continues its growth until it reaches the input voltage plus the clamp level V_{clp}. At this moment, the clamp diode conducts as shown in **Figure 2a**. As the drain node voltage becomes stuck at V_{in} + V_{clp}, the leakage current no longer flows in C_{lump} but exclusively in V_{clp}. The charge of the lump capacitor has absorbed energy from the leakage inductance and the current now circulating in V_{clp} is slightly less than the original peak primary current.

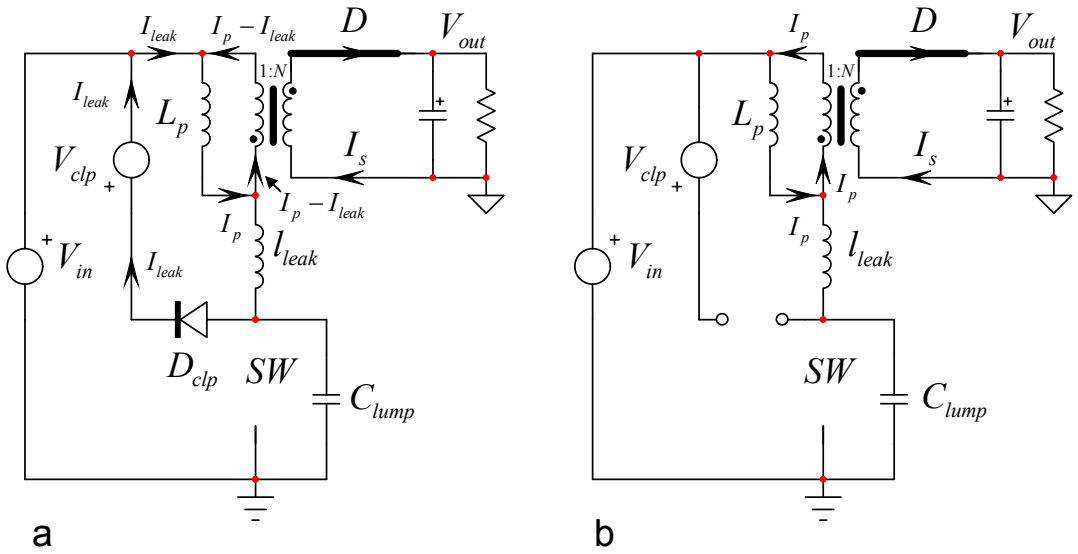

Figure 2: The clamp diode conducts when the lump capacitor is charged to V_{in} + V_{clp}.

When the switch opens with a peak current I_{p1}, the total energy stored in the circuit is equal to

$$W_{tot1} = \frac{1}{2}\left(L_p + l_{leak}\right) I_{p_1}^{\ 2} \tag{6}$$

The energy stored in the lump capacitance when the clamp diode begins conduction equals

$$W_{C_{lump}} = \frac{1}{2} C_{lump} \left(V_{in} + V_{clp} \right)^2 \tag{7}$$

At this moment, the energy stored in the circuit now involves the lump capacitance:

$$W_{tot2} = \frac{1}{2} \left(L_p + l_{leak} \right) I_{p_2}{}^2 + \frac{1}{2} C_{lump} \left(V_{in} + V_{clp} \right)^2 \tag{8}$$

in which I_{p2} is the circulating current after charging the lump capacitance. The quantity of energy described by (6) does not change except that part of it has been transferred to C_{lump}. Therefore,

$$W_{tot1} = W_{tot2} \tag{9}$$

Rearranging

$$\frac{1}{2} \left(L_p + l_{leak} \right) I_{p_1}{}^2 = \frac{1}{2} \left(L_p + l_{leak} \right) I_{p_2}{}^2 + \frac{1}{2} C_{lump} \left(V_{in} + V_{clp} \right)^2 \tag{10}$$

Solving for I_{p2} in this expression leads to

$$I_{p2} = \sqrt{I_{p1}{}^2 - \frac{C_{lump}}{l_{leak} + L_p} \left(V_{in} + V_{clp} \right)^2} \tag{11}$$

Assuming the following values

$l_{leak} = 12\ \mu\text{H}\ \ L_p = 600\ \mu\text{H}\ \ I_p = 1\ \text{A}\ C_{lump} = 150\ \text{pF}$
$V_{out} = 19\ \text{V}\ \ V_f = 1\ \text{V}\ \ N = 0.25\ \ V_{in} = 330\ \text{V}\ \ V_{clp} = 110\ \text{V}$

then (11) returns a current of 976 mA approximately or a reduction of 2.4% compared to the original 1-A peak current at the switch opening. Please note that C_{lump} is a highly non-linear term, especially at low voltages when the switch opens. If (11) is an approximate theoretical formula, bench experiments confirm the lower current circulating in the clamping network when diode D_{clp} starts conducting. Increasing the capacitance on the drain with an additional 100-pF capacitor (1 kV for offline applications) will reduce that current further. This extra capacitor helps for the *RCD* clamp temperature and benefits the turn-off losses by snubbing the drain voltage. EMI will also be improved by reducing the dV/dt on that node. However, adding that capacitor can potentially hamper the high-line turn-on losses budget if the operating frequency is high. A tradeoff must be found here.

At this point, the leakage inductance voltage is fixed (neglecting ripple): the lower terminal is stuck to $V_{in} + V_{clp}$ (neglecting the clamp diode drop) while its upper terminal is equal to $V_{in} + \frac{V_{out} + V_f}{N}$. The voltage applied across the leakage inductance is thus $V_{clp} - \left(V_{out} + V_f \right) / N$. The reset time of the leakage inductance begins here. The current defined in (11) drops with a slope equal to

$$S_{off,l_{leak}} = -\frac{V_{clp} - \frac{V_{out} + V_f}{N}}{l_{leak}} \tag{12}$$

As the leakage inductance resets, current in the secondary side diode $i_d(t)$ builds up at a slope defined by (12) but positive this time and scaled by the turns ratio. When the leakage inductance is full depleted, the current in the output diode is at its peak (**Figure 2b**). The secondary current now goes down at a slope defined by (5). This downslope lasts until the switch is turned on again. This is the off-time note t_{off}. However, the current in the output diode cannot instantaneously return to 0. And the reason is the time needed to energize the leakage inductance: its current must jump to that of the primary inductance still coupled to the secondary. This is the time during which the switch current grows from 0 to the valley current I_v. When $I_{SW} = I_v$, all the primary current now flows in the power switch and the secondary-side diode is blocked. Two important comments can be inferred from these information

1. the secondary side diode keeps conducting for a time t_1 when the switch turns on. It is the time for the leakage current to grow from 0 to the valley current I_v. As the output diode still conducts during this short period of time, L_p keeps demagnetizing: the leakage inductance extends the secondary diode conduction time by $d_1 T_{sw}$. Despite the switch closure, the slope change in the primary inductance does not occur before the current in the leakage inductance reaches the valley current and diverts the entire flow to ground: the duty ratio D is reduced by d_1.

2. when the switch SW opens, the secondary diode net current in the secondary is zero as all the primary current is diverted by the leakage inductance charging C_{lump}. As the leakage inductance resets, the secondary current builds up and reaches its peak when reset is complete: the leakage inductance delays the occurrence of the secondary current by the time t_2 and affects its peak value. The energy stored in the leakage inductance plus the extra energy stolen from the primary inductance are dissipated in the clamping network.

A close-up on this event appears in **Figure 3**. As you can see, the delay action of the leakage inductance is clear and prevents the secondary current from immediately reaching its peak. Furthermore, this peak current is not I_{peak}/N but as shown in [1] is equal to

$$I_{d,peak} = \frac{I_{peak}}{N}\left(1 - \frac{l_{leak}}{L_p}\frac{1}{\frac{NV_{clp}}{V_{out}+V_f} - 1}\right) \tag{13}$$

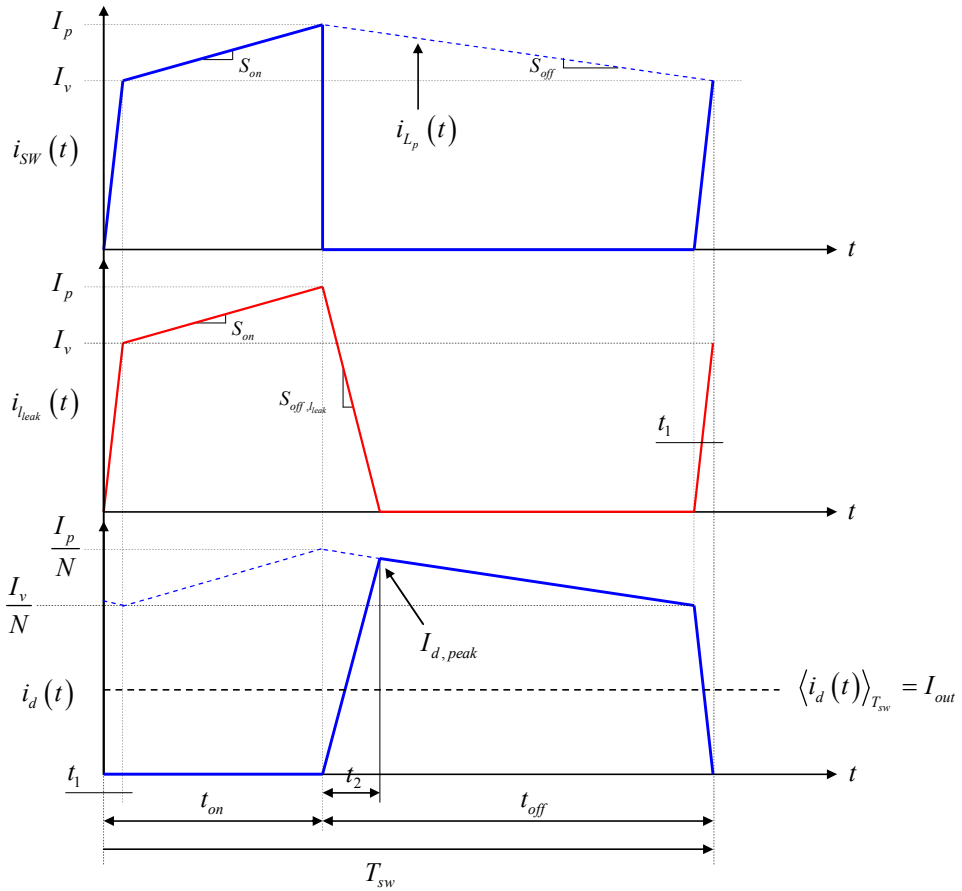

Figure 3: The secondary-side current peaks when the leakage inductance is depleted.

Updating the Dc Transfer Function

Now that we have a better understanding of what is going on during the transitions, let's compute the small time events we have described, t_1 and t_2. t_1 is the time needed to energize the leakage inductance from 0 to the valley current I_v. When SW closes, the voltage applied across the leakage inductance is the reflected output voltage (diode D still conducts) in series with the input voltage V_{in}. Neglecting the secondary-side diode forward drop V_f, the time t_1 is thus defined as:

$$t_1 = \frac{I_v l_{leak}}{V_{in} + \frac{V_{out}}{N}} \tag{14}$$

If we normalize it to the switching period, we obtain a duty ratio d_1 equal to

$$d_1 = \frac{I_v l_{leak}}{\left(V_{in} + \frac{V_{out}}{N}\right) T_{sw}} \tag{15}$$

The leakage inductance reset time t_2 is determined in a similar manner. The voltage applied across the leakage term when the switch opens (neglecting the lump capacitor charging time) is the clamping level V_{clp} minus the reflected voltage since D begins conducting. We thus have

$$t_2 = \frac{I_p l_{leak}}{V_{clp} - \frac{V_{out}}{N}} \tag{16}$$

Once normalized to the switching period, we obtain a duty ratio d_2 equal to

$$d_2 = \frac{I_p l_{leak}}{\left(V_{clp} - \frac{V_{out}}{N}\right) T_{sw}} \tag{17}$$

To determine the output voltage of a converter, a good tool is the inductor volt-second balance law which states that the average voltage across an inductor L at steady-state is 0:

$$\left\langle v_L(t) \right\rangle_{T_{sw}} = 0 \tag{18}$$

The voltage across the primary inductance follows the graph shown in **Figure 4**. To satisfy (18), we can write the following equation

$$\left\langle v_{L_p}(t) \right\rangle_{T_{sw}} = V_{in} \frac{L_p}{L_p + l_{leak}} (D - d_1) - \frac{V_{out}}{N} (1 - D + d_1) = 0 \tag{19}$$

Solving for V_{out} in the above expression and rearranging leads to

$$\frac{V_{out}}{V_{in}} = \frac{(D - d_1) L_p N}{(1 - D + d_1)(L_p + l_{leak})} = \frac{D - d_1}{1 - D + d_1} N \frac{L_p}{L_p + l_{leak}} \tag{20}$$

which simplifies to

$$\frac{V_{out}}{V_{in}} = \frac{ND}{1 - D} \tag{21}$$

when the leakage inductance is 0.

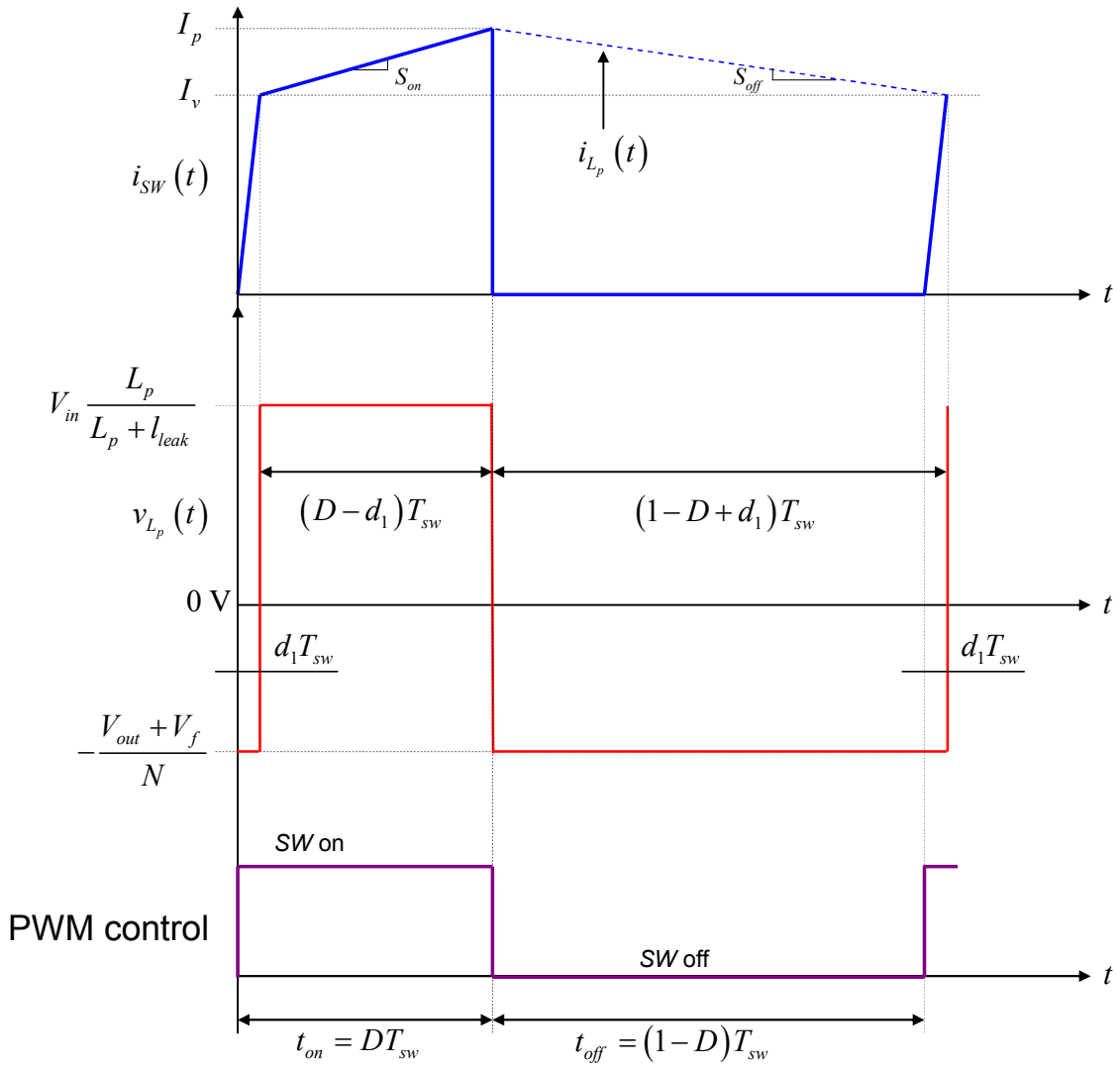

Figure 4: The primary inductance average voltage is 0 at steady-state.

What is interesting to observe is the fact that the effective on-time – the time during which the primary inductance slope is positive – is actually DT_{sw} reduced by d_1T_{sw}. This effective duty ratio further shrinks as the leakage inductance increases. The voltage applied across the primary inductance is also not V_{in} but less as expressed by (1).

A Simple Cycle-by-Cycle Model

To test our calculations and waveforms, we have captured a simple flyback converter operated at a 40% duty ratio and delivering slightly more than 60 W. The electrical diagram appears in **Figure 5**. The leakage inductance has been set to 50 µH, illustrating a badly-coupled transformer if you consider a 600-µH primary inductance (8.3%).

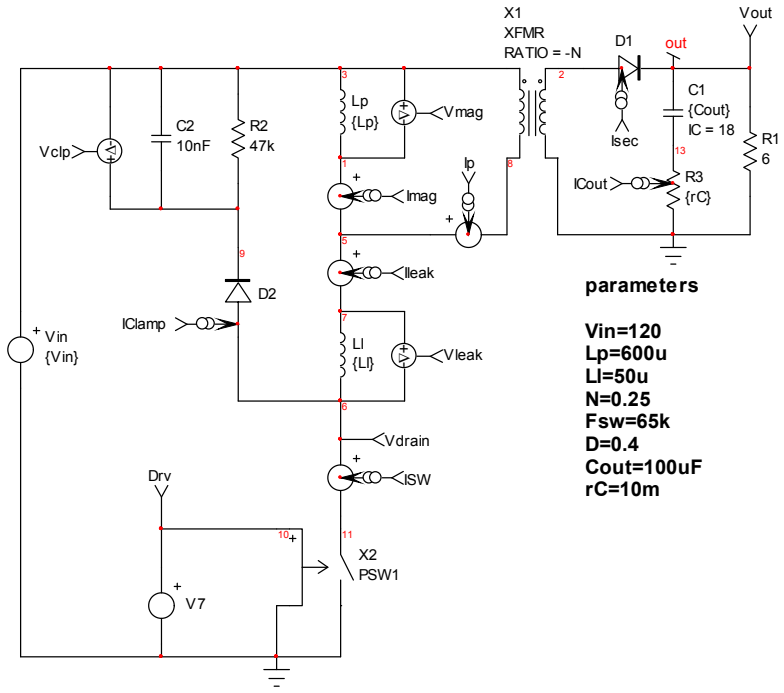

Figure 5: This simple model helps simulate a flyback converter and unveils its basic waveforms.

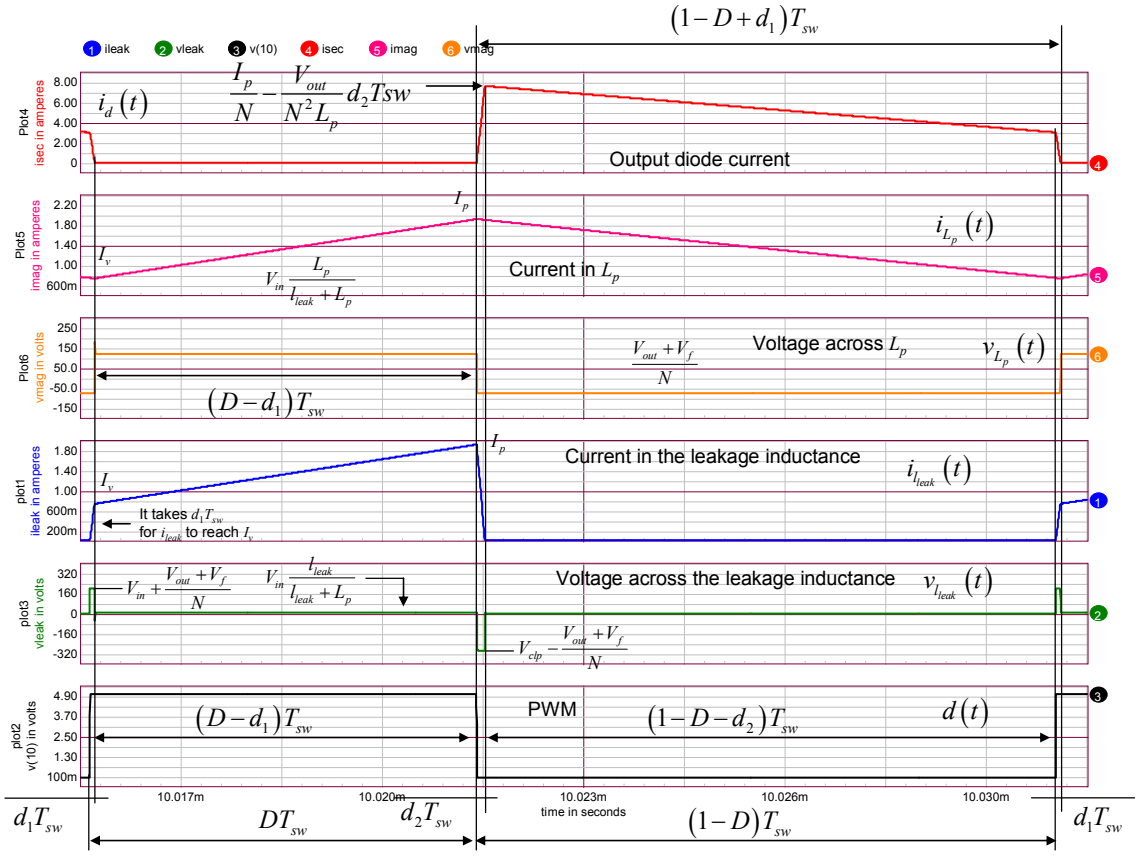

Figure 6: These waveforms show all the events we have described in the above lines.

From simulation, we can extract the following operating points in which V_{clp} is the voltage across C_2:

$I_p = 1.77$ A

$I_v = 672$ mA

$V_{clp} = 528$ V

The leakage inductance magnetizing time as described by (14) is measured to 176 ns. With a 65-kHz switching frequency, the d_1 duty ratio is thus

$$d_1 = 176n \times 65k = 1.14\% \tag{22}$$

Theoretically, with a transformer turns ratio N of 0.25, the output voltage of this flyback converter is equal to 20 V as defined by (21). If we apply (20) instead, the output voltage should actually be equal to

$$V_{out} = \frac{0.4 - 0.0114}{1 - 0.4 + 0.0114} \times 0.25 \times 120 \times \frac{600u}{600u + 50u} \approx 17.6 \text{ V} \tag{23}$$

The simulated output voltage appears in **Figure 7** and confirms this value. Please note that the diode we used in simulation has a forward drop equal to 0 V. You obtain this result by setting the diffusion parameter N to 10m in the diode model.

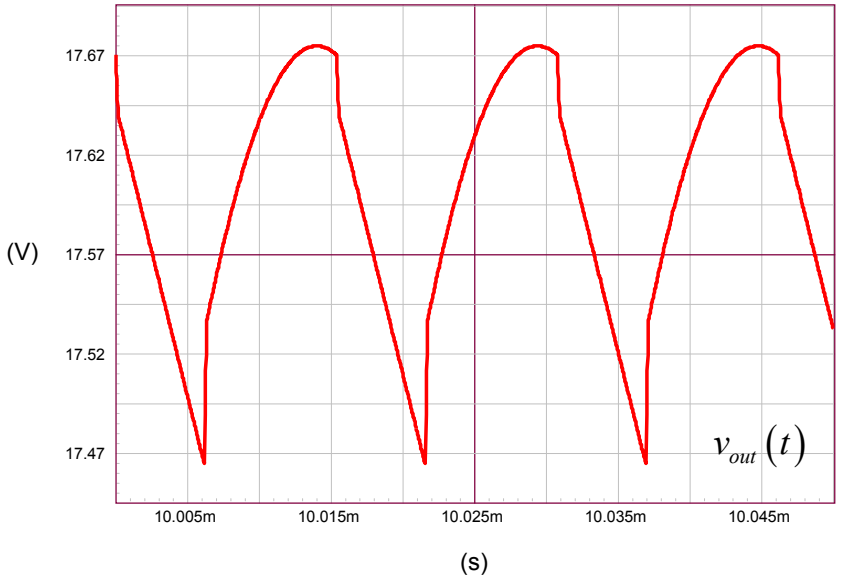

Figure 7: These waveforms show all the events we have described in the above lines.

The output current can also be precisely calculated knowing the leakage inductance reset time. Simulations give a valley current of 672 mA while the peak is 1.77 A. Applying (16) and considering a 528-V clamp voltage (the voltage across C_2 in **Figure 5**), the leakage inductance reset time is equal to

$$t_2 = \frac{1.77 \times 50u}{528 - \frac{17.57}{0.25}} = 193 \text{ ns} \tag{24}$$

and corresponds to a duty ratio of

$$d_2 = 193n \times 65k = 1.26\% \tag{25}$$

We can also estimate the secondary peak current when the leakage inductance is reset, 193 ns after the switch has turned off. Applying (13), we find

$$I_{d,peak} = \frac{1.77}{0.25}\left(1 - \frac{50u}{600u}\frac{1}{\frac{0.25\times 528}{17.57} - 1}\right) \approx 7 \text{ A} \tag{26}$$

From **Figure 3** low-side waveform, we can now determine the average current circulating in the diode and in the load by calculating the various areas constituting the curve:

$$\left\langle i_d(t)\right\rangle_{T_{sw}} = \frac{1}{2} I_{d,peak} d_2 + \frac{I_{d,peak} + \frac{I_v}{N}}{2}\left(1 - D - d_2\right) + \frac{1}{2}\frac{I_v}{N} d_1 \tag{27}$$

Applying numerical values, we have

$$\left\langle i_d(t)\right\rangle_{T_{sw}} = 0.5\times 7\times 0.0126 + \frac{7 + \frac{0.672}{0.25}}{2}\left(1 - 0.4 - 0.0126\right) + 0.5\times\frac{0.672}{0.25}\times 0.0114 = 2.9 \text{ A} \tag{28}$$

This is the value given by the waveform viewer as shown in **Figure 8**.

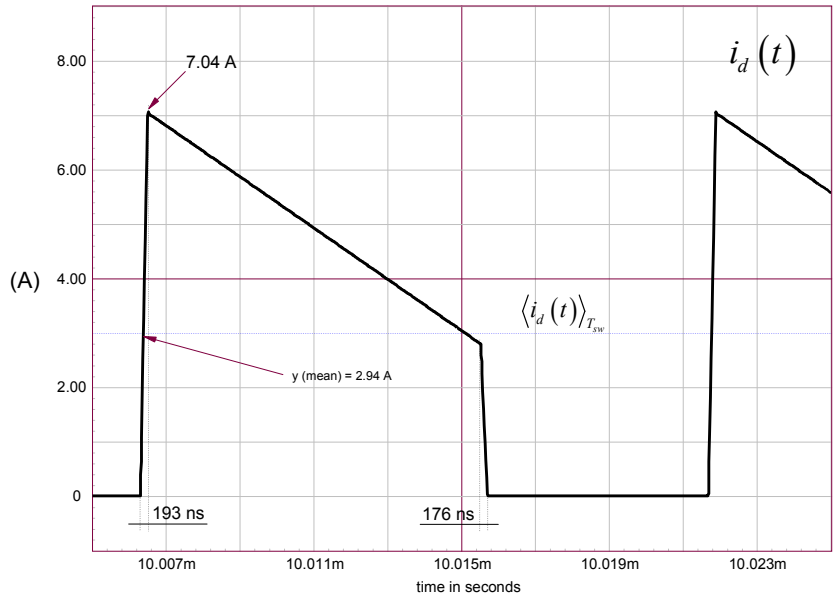

Figure 8: The simulated secondary side average current depends on the peak value but also on the various small duty ratios d_1 and d_2.

Hardware Verifications

To confirm our analysis, we have built simple fixed-duty ratio flyback converter whose leakage inductance has been artificially grown to 2.5% of the primary inductance by adding an external inductor. **Figure 9** shows the voltage on the MOSFET drain and the current in the secondary-side diode. As expected, the current does not instantaneously increase in the secondary when the switch opens. This is the delay brought by the leakage inductance demagnetization time. In the right side of the picture, you see that the diode waveform is slightly behind the drain voltage going down sharply. This is the leakage inductance magnetization time from 0 to the valley current. The close-up of **Figure 10** confirms a 62-ns conduction

time. The MOSFET turn-on event is well synchronized with the falling of $v_{DS}(t)$, but the magnetization cycle for L_p truly begins 62 ns later. During these 62 ns, L_p keeps demagnetizing despite the fact that the MOSFET has been turned on. This phenomenon is quite short here and can obviously be neglected. However, you can clearly observe the delay which will get significantly longer with an active clamp architecture.

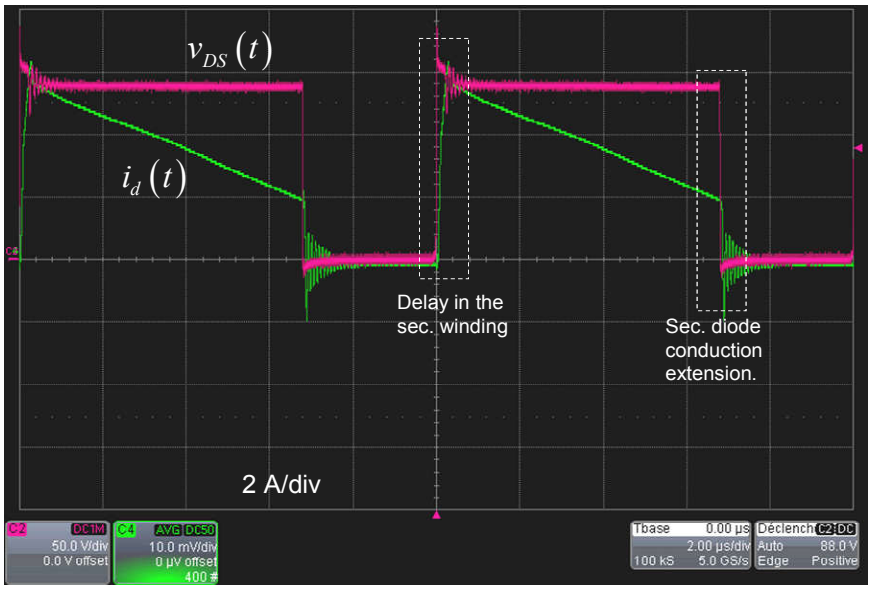

Figure 9: Waveforms captured on a prototype show the delay in the secondary side but also the small secondary diode conduction time extension.

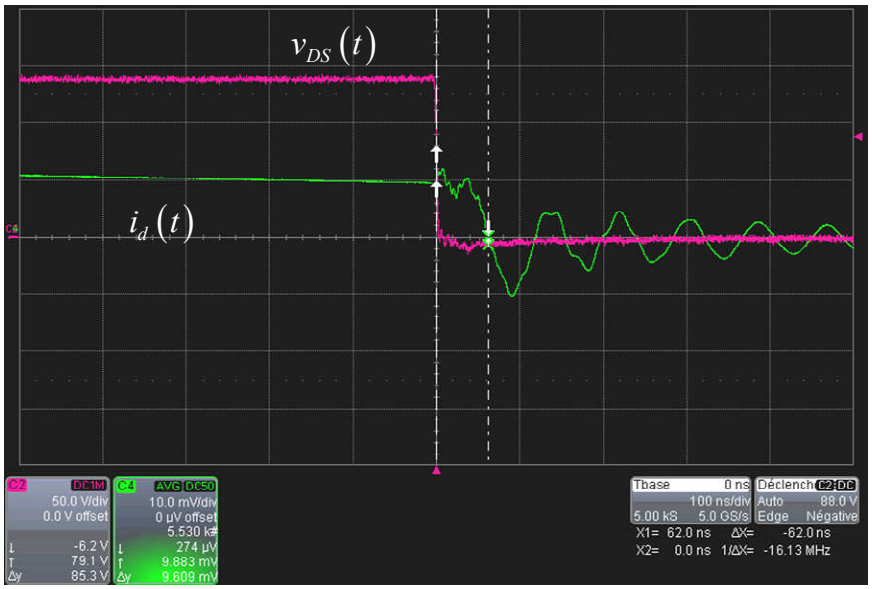

Figure 10: A close-up on the falling edge shows an extended duration of 62 ns for the secondary-side diode.

In **Figure 11**, you can clearly see the delay in the secondary side current but you can also evaluate the leakage inductance reset time. It is the time during which the drain voltage plateaus after the switch opening event. This event lasts 217 ns in this example. The overshoot can be quite significant and depends on the clamp diode forward transit time. It must be accounted for when assessing the worst-case margin you have on the MOSFET BV_{DSS}. When the *RCD* diode blocks, a high-frequency ringing involving the leakage inductance and C_{lump} occurs. It is sometimes necessary to damp these oscillations as they can

severely radiate and affect the EMI signature. Make sure the loop involving the *RCD* clamp is extremely short and kept close to the transformer. A series resistance with the diode of a few tens of ohms helps damping these oscillations.

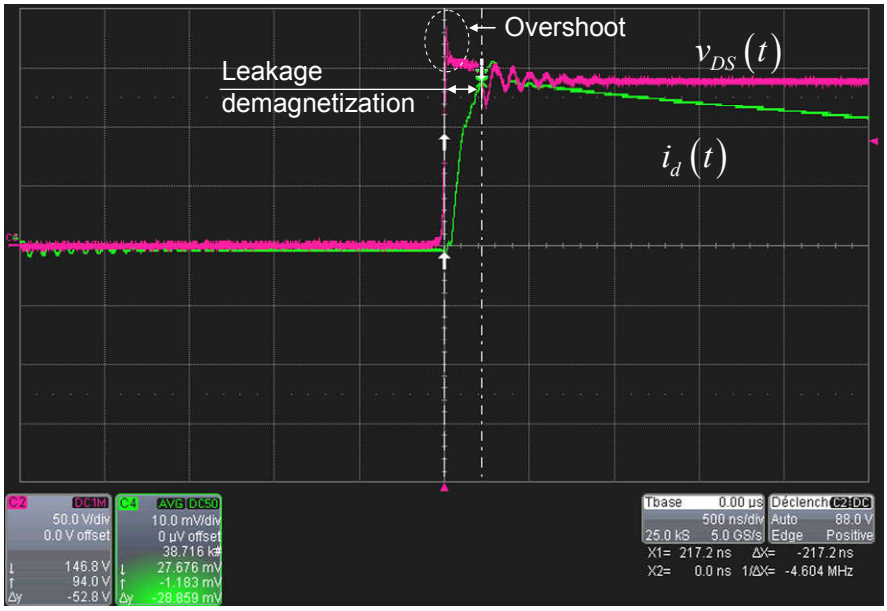

Figure 11: Observing the drain voltage reveals interesting information, in particular the leakage inductance reset time.

In this oscilloscope shot, the delay lasts a short period of time as the leakage inductance is quickly reset. In an active clamp converter, however, a resonance involving l_{leak} and C_{clamp} occurs at turn off, naturally expanding the reset along the off time. This resonance induces a smooth discontinuous waveform in the secondary despite a CCM operation.

Conclusion

This first part shows how flyback converter waveforms are affected by the leakage inductance. The effective duty ratio is reduced by the time needed to energize the leakage inductance while the demagnetization time of the primary inductance is extended by the same amount. The dc transfer function is affected and a new expression has been derived. These events are small in a flyback converter and can be difficult to visualize with a well-coupled transformer. However, in an active clamp converter, they can be of significant duration. Our next part will focus on the small-signal effects brought by the leakage inductance.

Note: thank you to Mark Pieper from T.I. who kindly pointed out an error in equation (6) which lead to a correction of the final clamp current definition.

References

1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, second edition, McGraw-Hill 2014, ISBN 978-0071823463

The Flyback Converter with Leakage Inductance
Part II – Average Modeling

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In the first part of this article, we have described the switching effects brought by the leakage inductance: a reduced effective duty ratio bringing an extension of the secondary diode conduction time and a delay in the secondary-side current appearance after the main switch has been turned off. As a result, the output voltage is lower than what the original formula predicts and power dissipation increases in the *RCD* clamping network. Given the impact brought by the leakage term in operating waveforms, it is interesting to investigate its influence on the small-signal response of the flyback converter. However, before we perform small-signal analysis, we need a good average model.

The Response to a Load Step

The cycle-by-cycle model introduced in part I appears in **Figure 1** and now includes a variable load. In this simulation, the load will vary from 8 to 6 Ω in a 10-µs span while the output is recorded. The converter runs in an open-loop configuration and we will increase the leakage inductance from 1 µH to 50 µH while the rest of operating parameters are kept constant (40% duty ratio).

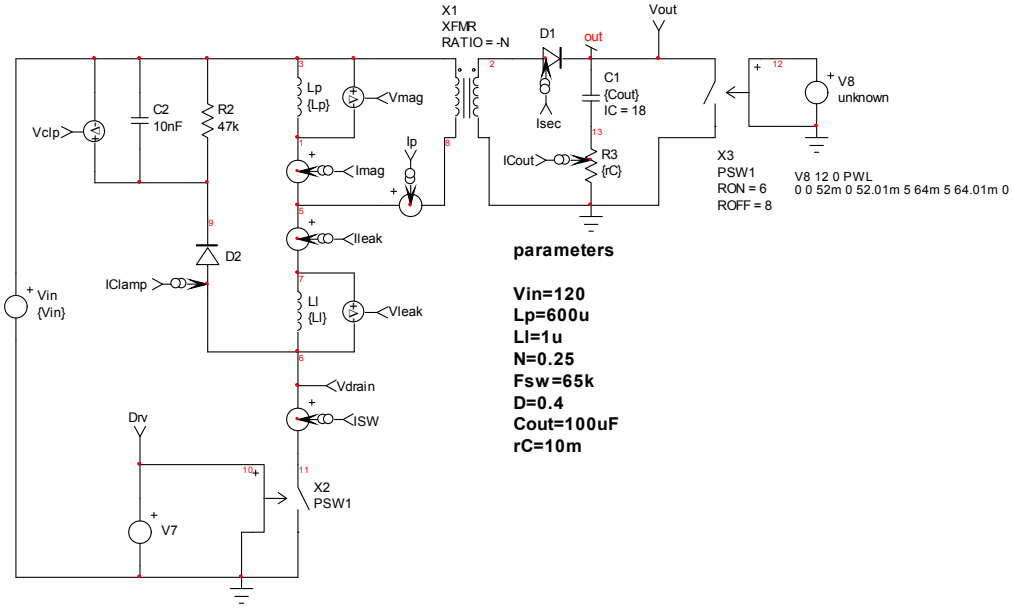

Figure 12: This open-loop simplified flyback converter will let us explore the effects brought by the leakage inductance.

We have gathered the output voltages obtained for various leakage inductances values in **Figure 13**. The vertical scale is 620 mV per division and common to each waveform but the offset is changed to let all curves enter the picture. The first comment pertains to the ringing. Without almost no leakage inductance (1 µH), the response rings and damping is light. However, the step in the load current does not affect the output voltage. As the leakage inductance grows, ringing starts to dampen and oscillations cease quickly for l_{leak} = 50 µH. However, the more leakage inductance you have, the lower the output voltage (from almost 20 V to 17.6 V) and the deeper the static voltage drop: almost 0 V with no leakage and up to 400 mV with the biggest leakage inductance. From this quick simulation, we can observe that the leakage inductance damps the transient response, affects the steady-state output voltage (as predicted in part I) but also degrades the output impedance. To explore the impact of the leakage inductance on the frequency response, we need a large-signal model later linearized to give a small-signal representation of our converter. From

this small-signal model, we should be able to analytically express the control-to-output transfer function of the flyback converter affected by a leakage inductance.

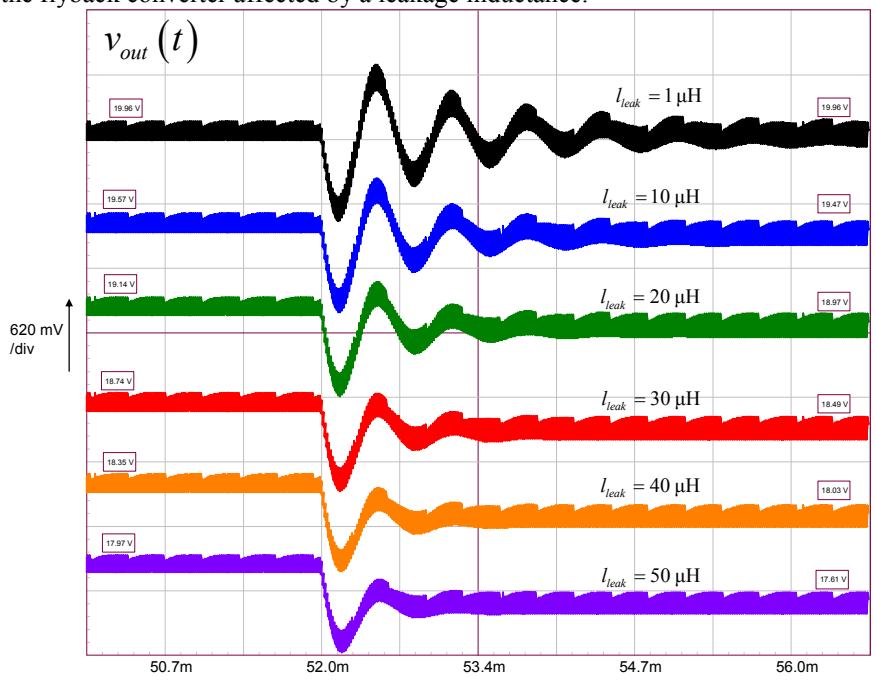

Figure 13: Varying the leakage inductance affects several parameters of the open-loop flyback converter.

A Large-Signal Model

The PWM switch lends itself very well to modeling a flyback converter. Introduced by Dr. Vatché Vorpérian in the 90s [1], the simplest version to model the large-signal response of a two-switch voltage-mode dc-dc converter operated in CCM and fixed switching frequency appears in **Figure 14**. The principle consists of averaging the waveforms between the connecting terminals, "a" (active), "p" (passive) and "c" for common and of describing currents/voltages through a set of time-continuous equations. Vorpérian showed that configuring current and voltage sources as in **Figure 14** was similar to consider an ideal dc transformer connected to terminals a-c-p and affected by a turns ratio *d*, the duty ratio.

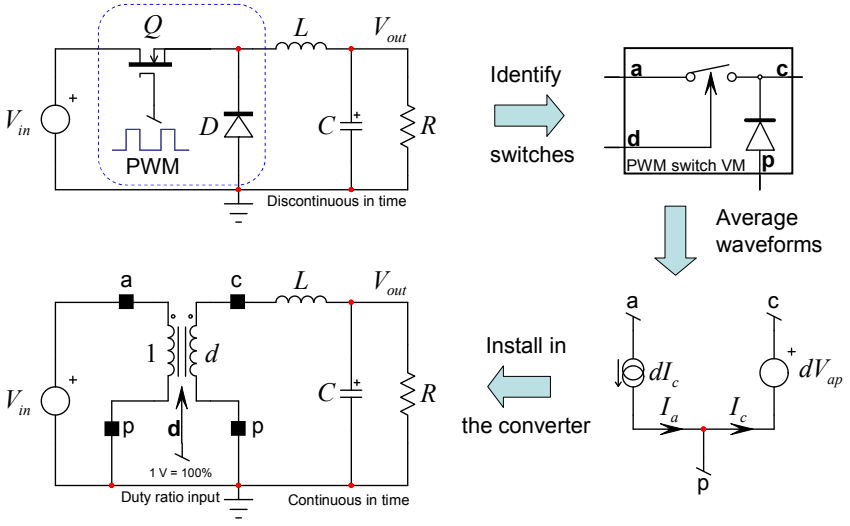

Figure 14: It is impossible to beat the PWM switch model in terms of simplicity!

The model is invariant meaning that it can be rotated to fit other dc-dc converters and all equations describing the PWM switch remain the same. The model presented in **Figure 14** is a large-signal version. If SPICE can deliver a small-signal response from this model – because SPICE is a linear solver it will linearize the model prior to running the simulation – we cannot use it as is to determine a control-to-output transfer function. We need a linearized or small-signal version of the PWM switch. It appears in **Figure 15** where you see the general architecture and how it translates into a working SPICE model. For those interested in further details of the PWM switch, [2] thoroughly covers the topic with a lot of working practical examples.

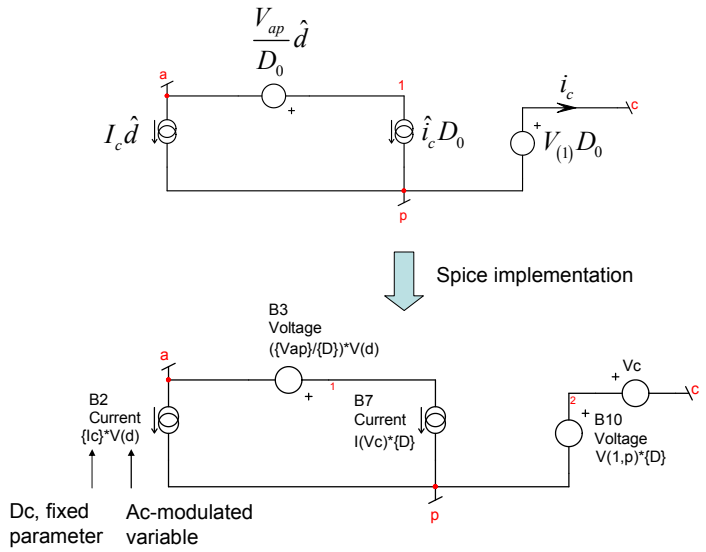

Figure 15: The small-signal version of the PWM switch slightly complicates the original model.

Please note that sources made of several terms associate products of dc and ac values. For instance, the series source B3 shows a fraction made of {Vap} over {D}, multiplied by V(d). {Vap} represents the steady-state voltage across terminals "a" and "p" while {D} is the steady-state duty ratio. These are fixed parameters and correspond to one operating point. For instance, {Vap} in the buck converter of **Figure 14** is V_{in}. d, the duty ratio can be any value between 0 and 1 V (0 to 100%). V(d) is the ac modulation (the $\hat{d}$) driving the model.

Figure 16 shows how you simulate a flyback converter using the PWM switch model and its equivalent with the special transformer of ratio 1:d. The framed voltages are the bias points calculated by the simulator. It is important to verify that they are within adequate limits. Sometimes the solver fails to determine the right operating point but a dynamic response is available. It is obviously a wrong result and you must discard it until a new correct operating point is found. From part I, we know that the perfect (no leakage inductance) dc transfer function of the CCM flyback is

$$V_{out} = V_{in}\frac{ND}{1-D} = 120 \times \frac{0.25 \times 0.4}{1-0.4} = 20 \text{ V} \qquad (1)$$

This is what the schematic displays across the load resistance: our bias point is correct. Now that we have a large-signal model, we can unveil the small-signal implementation built on what has been presented in **Figure 15**. For this purpose, we need to calculate a few of the fixed parameters, V_{ap} and the average current in terminal "c", I_c. Once you have rotated the PWM switch model to fit the flyback converter structure, the voltage between terminals "a" and "p", V_{ap}, becomes equal to the input voltage V_{in} minus the reflected voltage, V_{out}/N (neglecting the secondary diode V_f). As this voltage is negative, we have

$$V_{ap} = V_{in} + \frac{V_{out}}{N} \tag{2}$$

The current in terminal "c" is the average current flowing in the primary inductance L_p. Part of this current circulates in terminal "a" during the on-time or dT_{sw} and leaves through terminal "p" during the off-time or $(1–d)T_{sw}$. **Figure 18** shows the typical instantaneous waveforms for terminals "a" and "c". From the application schematic in **Figure 16**, the average current in terminal "a" also circulates in the input source to creates P_{in}:

$$P_{in} = I_a V_{in} \tag{3}$$

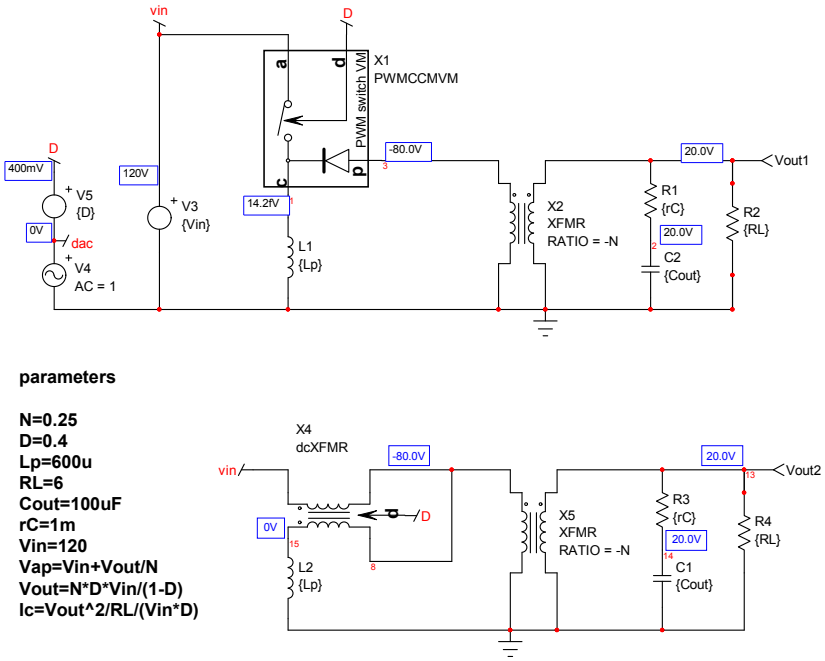

Figure 16: A practical implementation of the PWM switch model in a CCM flyback converter.

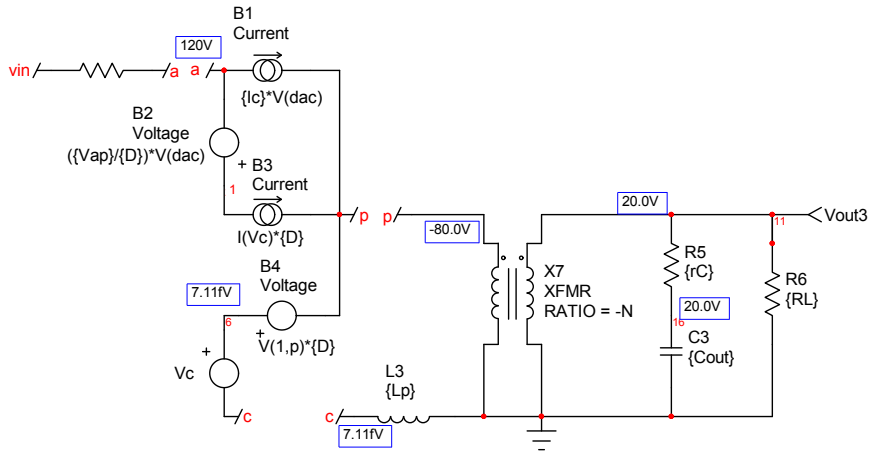

Figure 17: The small-signal version of the PWM switch model requires a few controlled sources only.

From **Figure 18**, we can write

$$I_a = dI_c \tag{4}$$

Substituting (4) in (3) and considering a 100% efficiency ($P_{in} = P_{out}$), we have

$$dI_c V_{in} = \frac{V_{out}^2}{R_L} \tag{5}$$

Thus

$$I_c = \frac{V_{out}^2}{R_L dV_{in}} \tag{6}$$

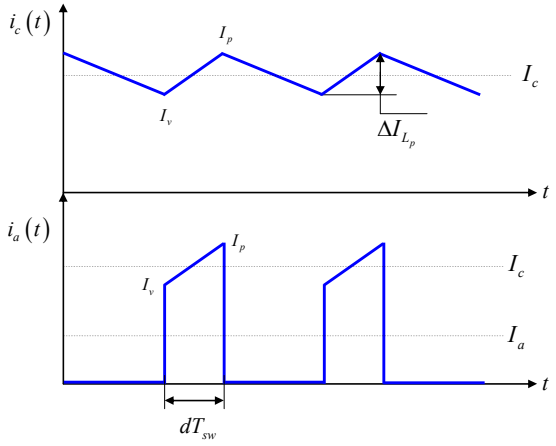

Figure 18: The current in terminal "c" is that of the primary inductance L_p.

This expression is evaluated in **Figure 16** parameters window and passed as a parameter to the controlled sources (values between curly braces). We can now run the simulation and gather all curves in a common graph. This is what we did in **Figure 19** and all curves (magnitude and phase) perfectly superimpose. This is the classical response of a CCM flyback converter from the duty ratio input to the output. There is a peaking at the resonant frequency, then the ESR (equivalent series resistance, r_C) zero kicks in, followed by the RHP (right half-plane) zero which brings the phase further down.

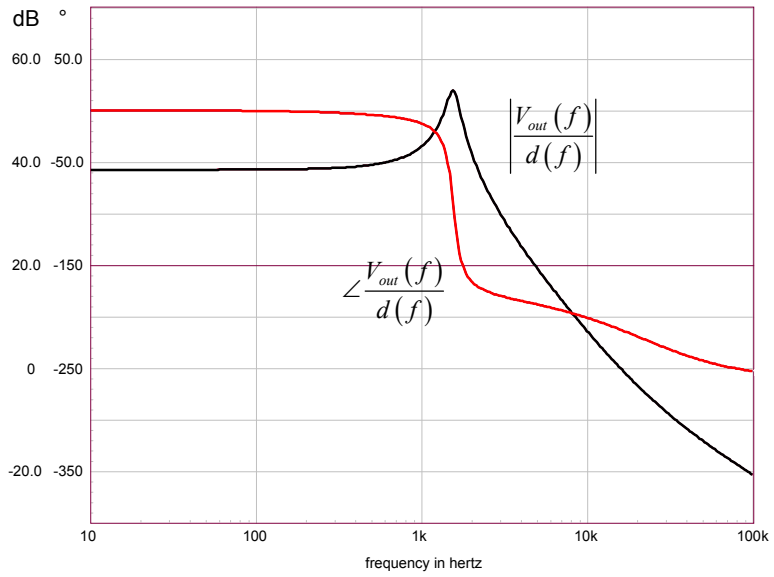

Figure 19: Frequency responses obtained from the 3 different models (encapsulated large-signal model, transformer-based circuit and the linearized version) perfectly superimpose.

Considering the Leakage Inductance

In the average model presented in **Figure 16**, the voltage applied to the model is V_{in}. This voltage biases the primary inductance L_p during dT_{sw}. In reality, as seen in part I, considering the leakage inductance, the voltage splits between the leakage and primary inductances forming a voltage divider *Div*:

$$Div = \frac{L_p}{L_p + l_{leak}} \tag{7}$$

The first upgrade to the model is to replace V_{in} by $V_{in} \times Div$. The second change involves the duty ratio d. We have seen in part I that the duty ratio was affected by the leakage inductance magnetization time $d_1 T_{sw}$. The effective duty ratio applied to the average model needs to reflect this fact and is given by

$$d_{eff} = d - d_1 \tag{8}$$

d_1 depends on the leakage inductance value by (neglecting the secondary-side diode drop V_f) and the valley current I_v.

$$d_1 = \frac{I_v l_{leak}}{\left(V_{in} + \frac{V_{out}}{N}\right) T_{sw}} \tag{9}$$

To calculate the valley current, we can look back at **Figure 18** and see that the valley current is actually the average current I_c minus half the primary inductance ripple:

$$I_v = I_c - \frac{\Delta I_{L_p}}{2} \tag{10}$$

The ripple current is the excursion brought by applying V_{in} over the series connection of L_p and l_{leak} during t_{on} or dT_{sw}. The valley current is thus

$$I_v = I_c - \frac{d_{eff} T_{sw} V_{in}}{2\left(L_p + l_{leak}\right)} \tag{11}$$

The peak current is obtained in a similar way except that you reach it by adding half of the inductor ripple to I_c rather than subtracting it as in the above:

$$I_p = I_c + \frac{d_{eff} T_{sw} V_{in}}{2\left(L_p + l_{leak}\right)} \tag{12}$$

The current circulating in the clamping network lasts $d_2 T_{sw}$, the leakage inductance reset time. This time depends on l_{leak} of course, but also from the reflected V_{out} and the clamp voltage V_{clp}. From part I we have determined the corresponding duty ratio as

$$d_2 = \frac{I_p l_{leak}}{\left(V_{clp} - \frac{V_{out}}{N}\right) T_{sw}} \tag{13}$$

Figure 20 represents the various currents at play during the on-time. The low-side is the power switch current and above it, the current in the leakage inductance. When the switch turns off, we have seen that almost immediately (neglecting C_{lump} charging time), the current diverts into the clamping network and quickly goes down to 0. At this moment, the leakage inductance is reset and the secondary current is at its peak.

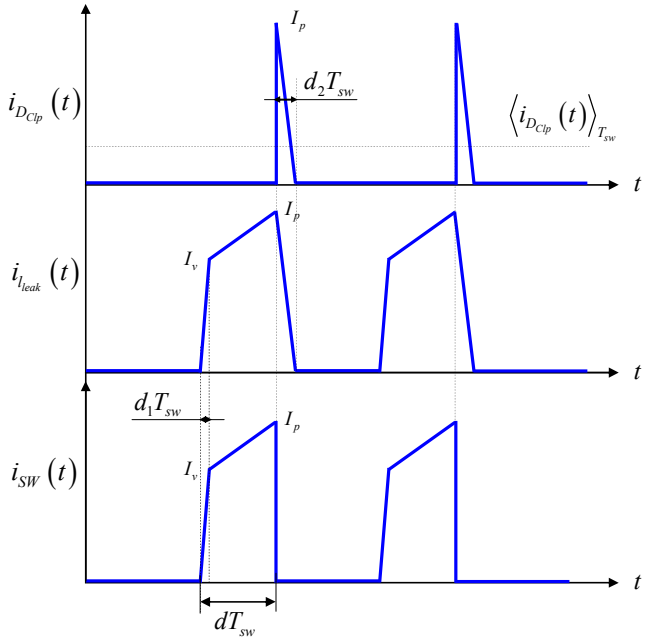

Figure 20: The current circulates in the *RCD* network during the leakage inductance reset time d_2T_{sw}.

The average current thus circulating in the clamp diode is simply the small triangle surface averaged along the switching cycle:

$$\left\langle i_{D_{Clp}}(t)\right\rangle_{T_{sw}} = \frac{1}{2} I_p d_2 \tag{14}$$

Since I_p is computed by (12), we can connect a *RC* network across the current source modeled by (14) and we will obtain an averaged clamp voltage. In SPICE, this voltage will be used to determine d_2 as described by (13). The peak current in this equation depends on the output voltage applied across the load resistance. This voltage depends on d_1 as seen in part I. When you run the simulation, SPICE ends up to solve a 6-unknow/6-equation system and can sometimes fail to determine the right answer. To help it converge to the right result, a .NODESET statement telling it what "seed" to use will efficiently lead to the right bias point. That seed is the clamp voltage that we can suggest to SPICE prior it runs. The final large-signal model appears in **Figure 21**. The added command line is .NODESET V(clp) = 300 V.

The exercise now consists of comparing the load-step response from the cycle-by-cycle model to that of the updated average model. Several leakage inductance values are selected, 1 µH, 10 µH and 30 µH. As confirmed by **Figure 22**, **Figure 23** and **Figure 24**, the agreement between the cycle-by-cycle model and the average version is excellent. The left-side of these figures shows the large-scale response while the right side shows a zoomed version confirming how well the averaged version tracks the switched model. A small discrepancy occurs in the clamp voltage, particularly in the dc level. This voltage depends on the t_2 duration which can be of extremely small value. Any spread in the prediction of this parameter leads to a wide difference in the end. **Figure 25** compares voltages observed at the clamp diode cathode in both models. Both curves match well despite the small offset difference which introduces a 2.5% error in this case. This error increases as l_{leak} does but keeps well within 10% for large l_{leak} values.

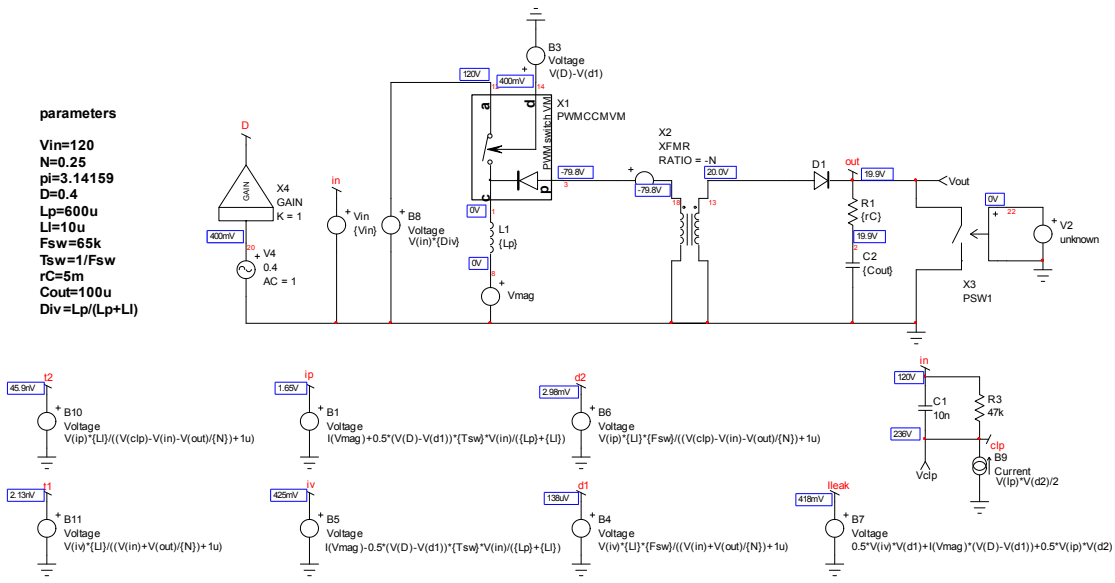

Figure 21: The updated large-signal model now includes the leakage inductance contribution.

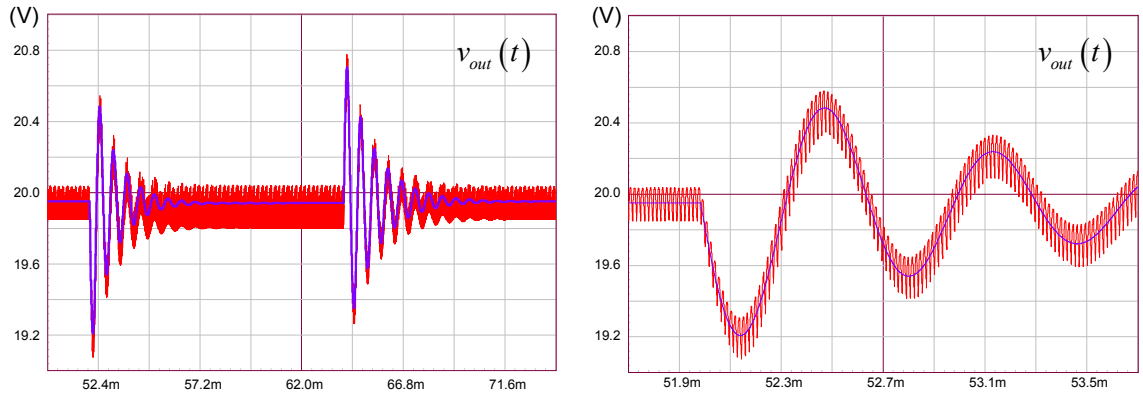

Figure 22: Transient response for a 1-µH leakage inductance.

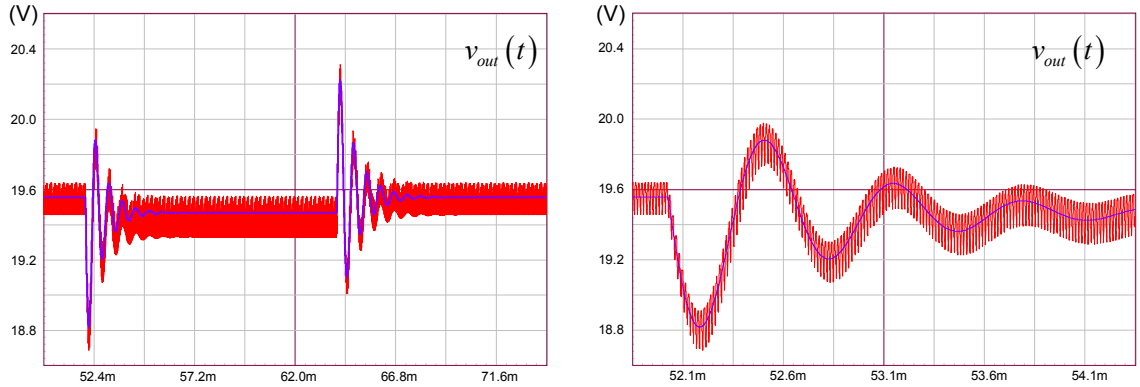

Figure 23: Transient response for a 10-µH leakage inductance.

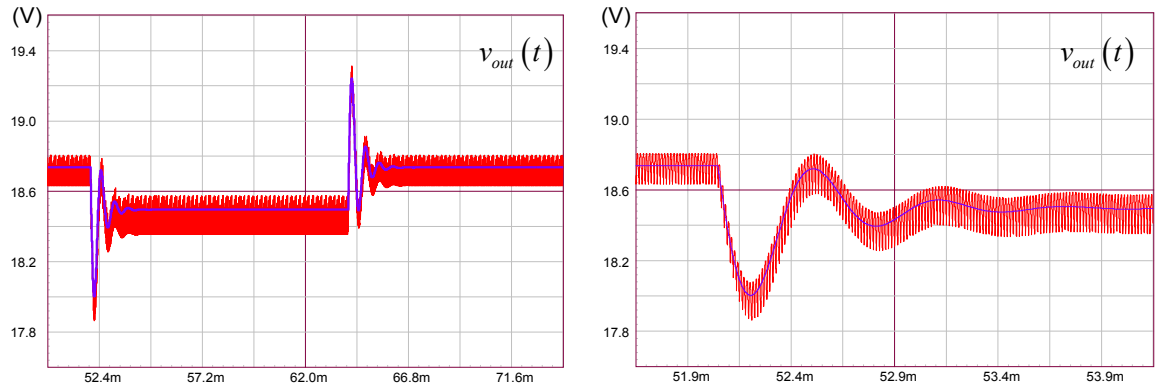

Figure 24: Transient response for a 30-µH leakage inductance.

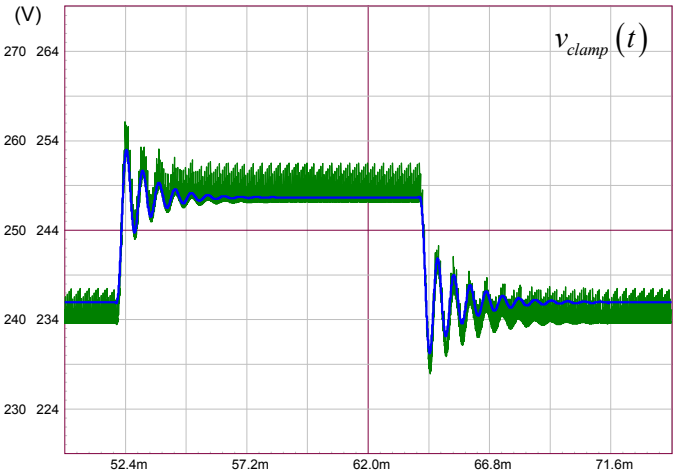

Figure 25: The averaged clamp voltage (on the clamp diode cathode) tracks fairly well the cycle-by-cycle version (l_{leak} = 1 µH).

These experiments confirm that the large-signal model accounting for the leakage inductance matches the cycle-by-cycle version quite well and can consequently be considered for the linearization exercise.

Conclusion

In this second part, we have seen how the leakage inductance damped the transient response of the flyback converter operated in CCM. Using the PWM switch model and including the leakage inductance contribution, we were able to build an average model mimicking the cycle-by-cycle version. This helped confirm that our approach was correct. It paves the way for the third and last part article in which we will derive the small-signal response of the converter.

References

1. V. Vorpérian, "Simplified Analysis of PWM Converters Using the Model of the PWM Switch, Parts I (CCM) and II (*DCM*), " *Transactions on Aerospace and Electronics Systems*, vol. 26, no. 3, *May* 1990
2. C. Basso, "Switch Mode Power Supplies: SPICE Simulations and Practical Designs", second edition, McGraw-Hill 2014, ISBN 978-0071823463

The Flyback Converter with Leakage Inductance
Part III – Small-Signal Modeling

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In the final part of this article series, we will study the small-signal response of the CCM flyback converter operated in voltage mode and affected by the leakage inductance. From the updated large-signal model introduced in part II, we will step-by-step progress through successively-simplified small-signal schematics with the goal to establish the simplest linear version. From this final circuit, we will extract the control-to-output transfer function for showing how the leakage inductance affects the quality factor of the transfer function denominator.

From Large to Small Signal

When you want to derive the transfer function of a complicated circuit, your aim is to reduce complexity so that analysis is carried over the simplest schematic. However, as you progress through the circuit reduction – by factoring terms, simplifying expressions, neglecting variables and so on – you must test your new circuit and compare its response to that of the original circuit, the one at the beginning of the exercise. Any deviation between the original response and what your next simplified version delivers indicates that you did a mistake or the assumption you made is overly simplistic: Discard the circuit and go back one step to rework it. By following these steps, you surely progress slowly but carefully as you immediately detect and correct mistakes. Experience teaches that nothing is more frustrating than identifying an error at the very end while you realize something was wrong at one of the intermediate steps!

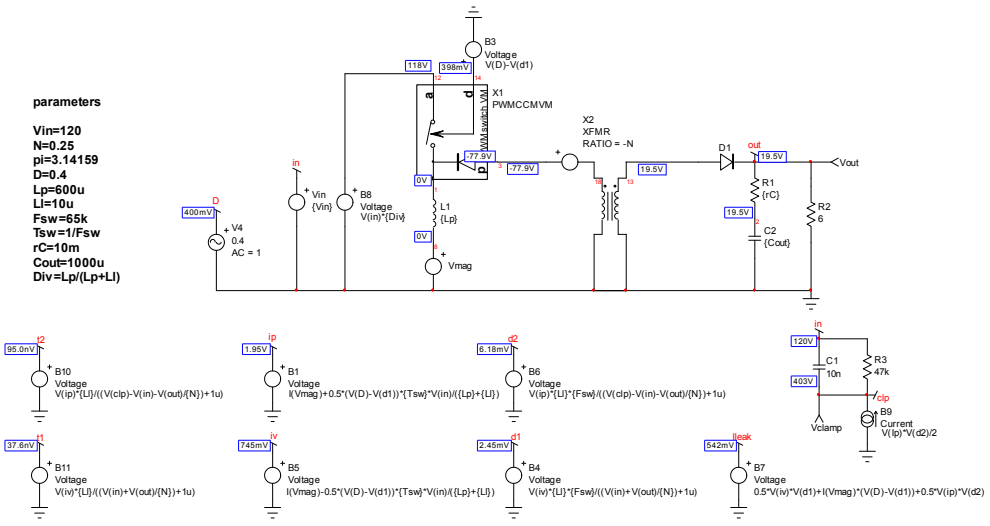


Figure 26: This open-loop large-signal schematic is our starting circuit and its dynamic response will serve as a reference for the following steps.

The first thing we can do is replace the large-signal PWM switch model by its small-signal version introduced in part II. Then, we can run an ac simulation and verify that operating points and responses are identical. The non-linear model is in **Figure 1** while the small-signal version appears in **Figure 27**. The duty ratio has been split into two sources, one for the static duty ratio and the second for the ac modulation; the $\hat{d}$ in the small-signal equations. Bias points are identical to those of **Figure 1** meaning that this first step is correct, dc-wise. Let's check how frequency responses of these two circuits compare. We have gathered Bode plots in **Figure 28**: magnitude and phase curves superimpose, validating our first step.

The circuit in **Figure 27** is correct but quite complicated. As stated, small-signal analysis implies simplifying the circuit as much as you can and rearranging the various components into a more meaningful

architecture. Please note that V_c and V_{mag} are dummy 0-V sources and probe the current leaving terminal "c".

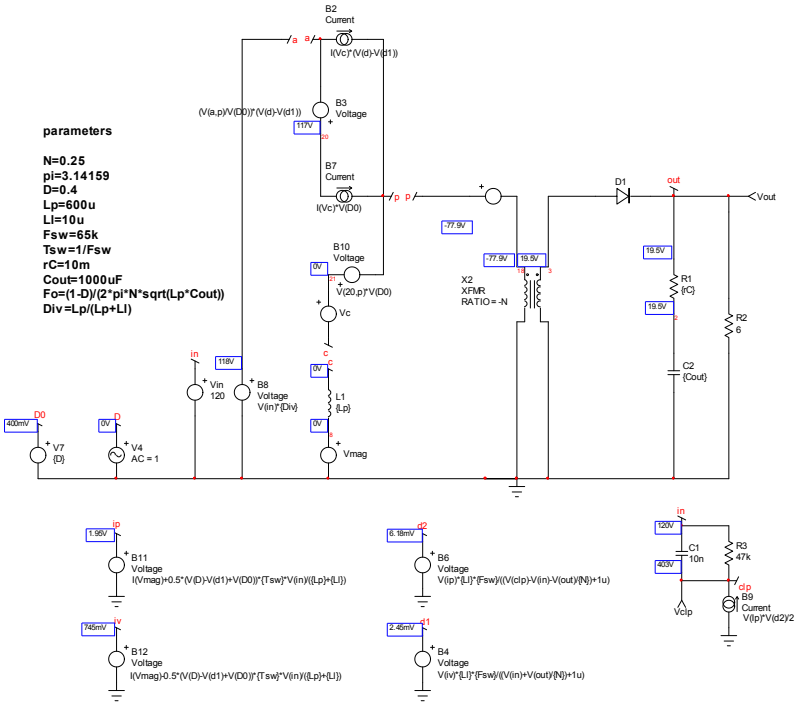


Figure 27: The PWM switch is replaced by its small-signal version and the circuit dynamic response is checked against the reference frequency response.

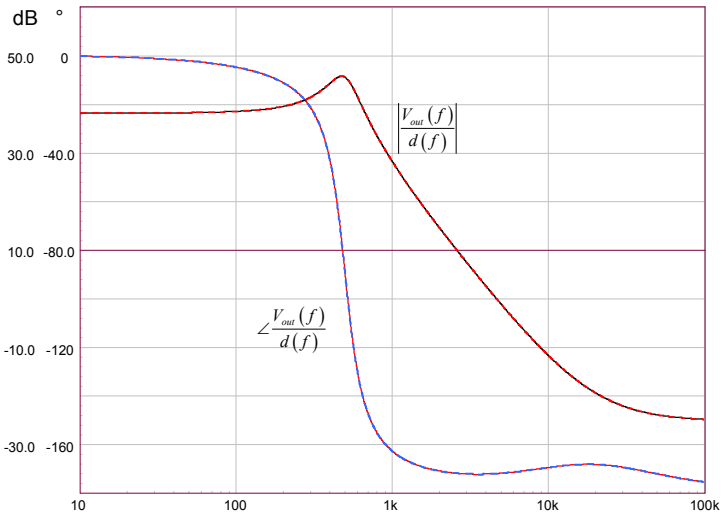


Figure 28: Bode plots of both circuits perfectly superimpose, validating this first step.

The PWM switch model we plugged is indeed a linearized version and we do not need to work on it. However, all the sources computing the peak and valley currents, the clamp voltage and so on are still large-signal expression that we need to linearize. Fortunately, some of these sources are not needed in our ac analysis such as I_p and d_2 for instance.

Sources Linearization

You have two options if you want to linearize these sources. You can perturb each variable with a small excitation – the little hat ^ you see on certain variables – and sort out ac and dc terms to form two separate equations: a static and a dynamic expression. The static expression describes the operating point while the dynamic expression is the one we want. The problem with this technique is the amount of terms and cross products you obtain, especially with more than two variables. Sorting these terms for forming ac and dc equations can sometimes be tedious and source of mistakes. Let's try with the valley current definition:

$$I_v = I_C - \frac{(d-d_1)V_{in}T_{sw}}{2(l_{leak}+L_p)} \tag{1}$$

There are three variables here, I_c, d and d_1. If we perturb each variable with a small quantity, we have

$$I_v + \hat{i}_v = I_C + \hat{i}_c - \frac{(d+\hat{d}-d_1-\hat{d}_1)V_{in}T_{sw}}{2(l_{leak}+L_p)} \tag{2}$$

Expanding leads to

$$I_v + \hat{i}_v = I_C + \hat{i}_c + d_1\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} - d\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} + \hat{d}_1\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} - \hat{d}\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} \tag{3}$$

Now collecting ac and dc terms, we have two definitions:

$$\begin{aligned} I_v &= I_C + d_1\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} - d\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} \\ \hat{i}_v &= \hat{i}_c + \hat{d}_1\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} - \hat{d}\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} \end{aligned} \tag{4}$$

If we define two coefficients k_{ivd} and k_{ivd1} as

$$k_{ivd} = -\frac{T_{sw}V_{in}}{2(L_p+l_{leak})} \tag{5}$$

$$k_{ivd1} = \frac{T_{sw}V_{in}}{2(L_p+l_{leak})} \tag{6}$$

the dynamic equation in (4) can be rearranged in a simpler format

$$\hat{i}_v = \hat{i}_c + \hat{d}_1 k_{ivd1} + \hat{d}k_{ivd} \tag{7}$$

Static coefficients k_{ivd} and k_{ivd1} will be passed as parameters in the schematic capture and evaluated before simulation begins.

The triage operation was simple here but with complex expressions and multiple variables, it quickly becomes a difficult exercise that you cannot automate under a solver like Mathcad®. A faster way consists of using partial differentiations given a set of uncorrelated (independent) variables as shown below:

$$di_v = \frac{\partial I_v(I_c,d,d_1)}{\partial I_c}di_c + \frac{\partial I_v(I_c,d,d_1)}{\partial d_1}dd_1 + \frac{\partial I_v(I_c,d,d_1)}{\partial d}dd \tag{8}$$

or using small-signal notation

$$\hat{i}_v = \frac{\partial I_v\left(I_c, d, d_1\right)}{\partial I_c}\hat{i}_c + \frac{\partial I_v\left(I_c, d, d_1\right)}{\partial d_1}\hat{d}_1 + \frac{\partial I_v\left(I_c, d, d_1\right)}{\partial d}\hat{d} \tag{9}$$

Here, coefficients for ac terms only are obtained from these partial differentiations. Applying this method to the d_1 generator in **Figure 27** gives

$$\hat{d}_1 = \frac{\partial d_1\left(I_v, V_{out}\right)}{\partial I_v}\hat{i}_v + \frac{\partial d_1\left(I_v, V_{out}\right)}{\partial V_{out}}\hat{v}_{out} \tag{10}$$

which leads to evaluating

$$\hat{d}_1 = \frac{\partial}{\partial V_{out}}\frac{I_v l_{leak} F_{sw}}{V_{in} + \frac{V_{out}}{N}}\hat{v}_{out} + \frac{\partial}{\partial i_v}\frac{I_v l_{leak} F_{sw}}{V_{in} + \frac{V_{out}}{N}}\hat{i}_v \tag{11}$$

Considering k_{d1vo} and k_{d1iv} coefficients, we can rewrite (11) as

$$\hat{d}_1 = k_{d1vo}\hat{v}_{out} + k_{d1iv}\hat{i}_v \tag{12}$$

in which

$$k_{d1vo} = -\frac{F_{sw} I_v l_{leak}}{N\left(V_{in} + \frac{V_{out}}{N}\right)^2} \tag{13}$$

$$k_{d1iv} = \frac{F_{sw} l_{leak}}{V_{in} + \frac{V_{out}}{N}} \tag{14}$$

Now that we have linearized d_1 and I_v sources, we can update and simplify **Figure 27** circuit. The result appears in **Figure 29**: expressions in (5), (6) and in (13) and (14) are calculated in the parameters text window. All sources in this diagram are now small-signal types. A quick ac analysis shows that the frequency response in magnitude and phase exactly matches that of **Figure 28**.

Simplifying the Schematic

We could start analyzing the linearized converter from this schematic. However, further simplifications and rearrangements are possible. For instance, in the control-to-output transfer function, the input voltage V_{in} is constant, meaning that $\hat{v}_{in}$ or $V_{in}(s)$ are equal to 0. As such, node "a" which is connected to the input voltage can be advantageously grounded. By grounding node "a", you can redraw the circuit and reveal a simpler version as in **Figure 30**. The frequency response of this circuit is tested against that of **Figure 28** to detect any error in the newly-arranged model.

Further observation shows that current source B_7 is in series with voltage source B_1. For the sake of simplifying further, B_7 negative terminal can be ground-referenced while B_1 is transformed into a separate source with its output connected to node 20. The new circuit is given in **Figure 31**. Node 20 is used in the B_{10} source (which is updated with its definition) and both current sources B_7/B_2 can be paralleled to form a single source. This is what is shown in **Figure 32** as a final circuit for the analysis. Please note that source I_v expression has been included into the d_1 source. The frequency response of this

circuit is plotted versus that of the large-signal reference model in **Figure 33**. As phase and magnitude responses are identical, we can now work on this final representation.

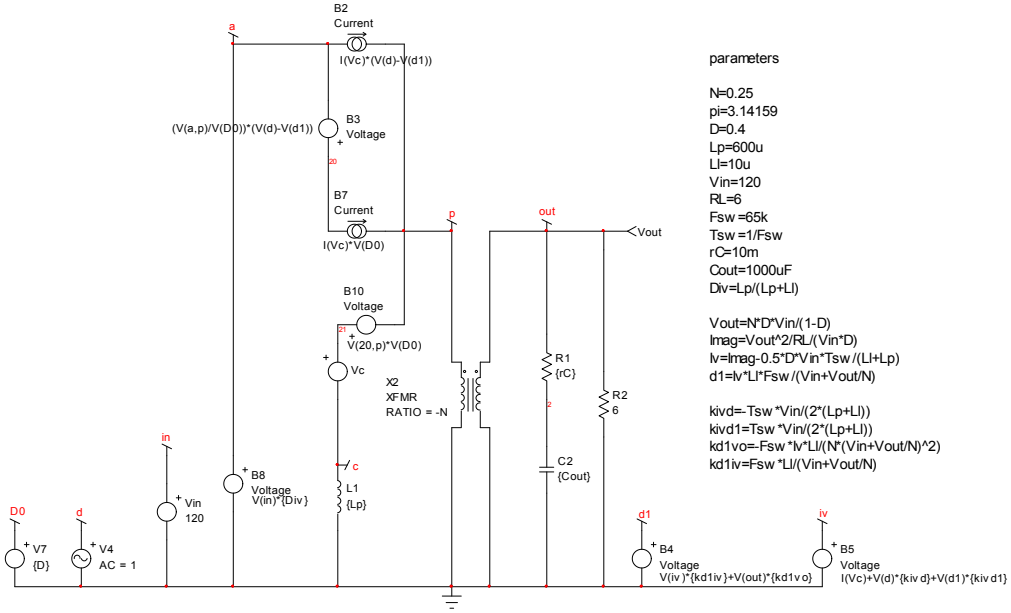


Figure 29: The updated circuit now includes linearized source only.

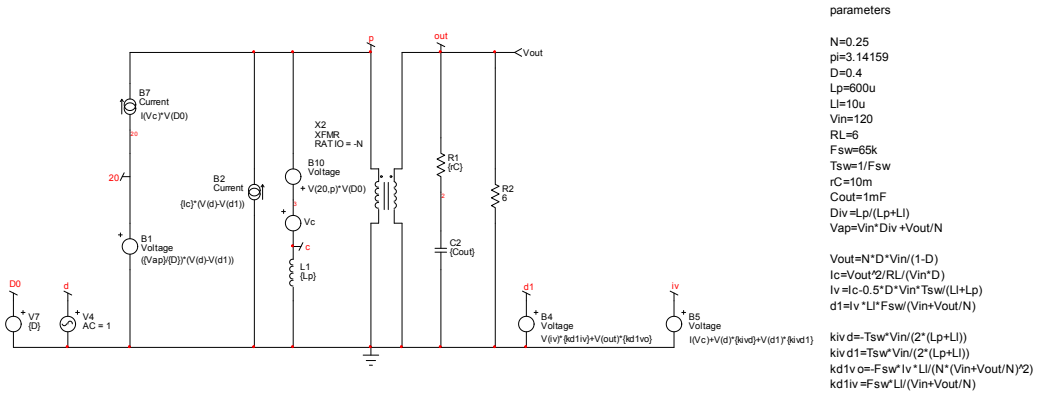


Figure 30: Considering a constant input voltage, node "a" can be grounded and further simplification brought to the small-signal circuit.

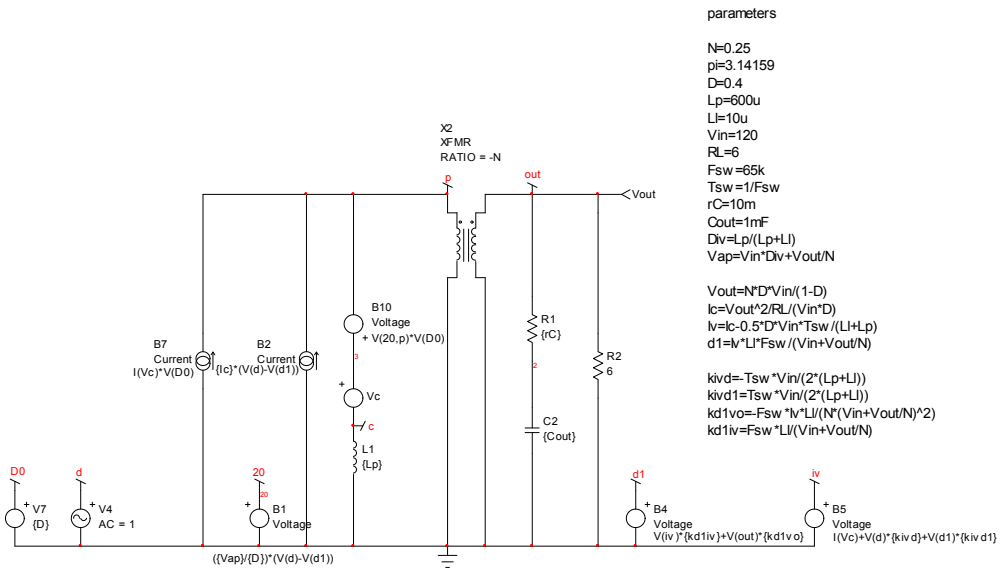


Figure 31: Current source B_7 is now grounded while B_1 delivers its voltage at node 20. V_c is a 0-V dummy source probing the current in the primary inductance.

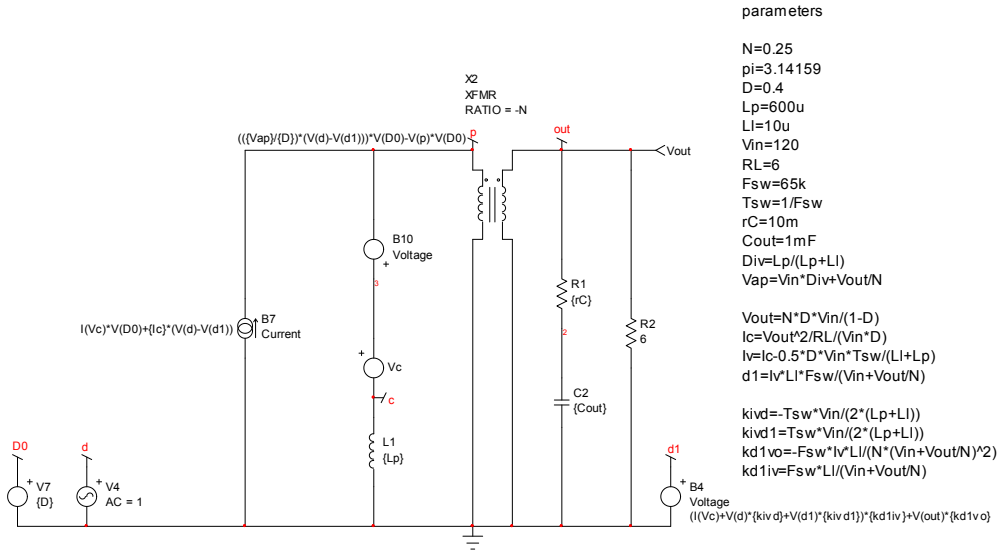


Figure 32: Once current source B_2 in **Figure 31** has been included into B_7 and node 20 integrated into B_{10}, we have our final small-signal schematic. I_v has been incorporated into d_1.

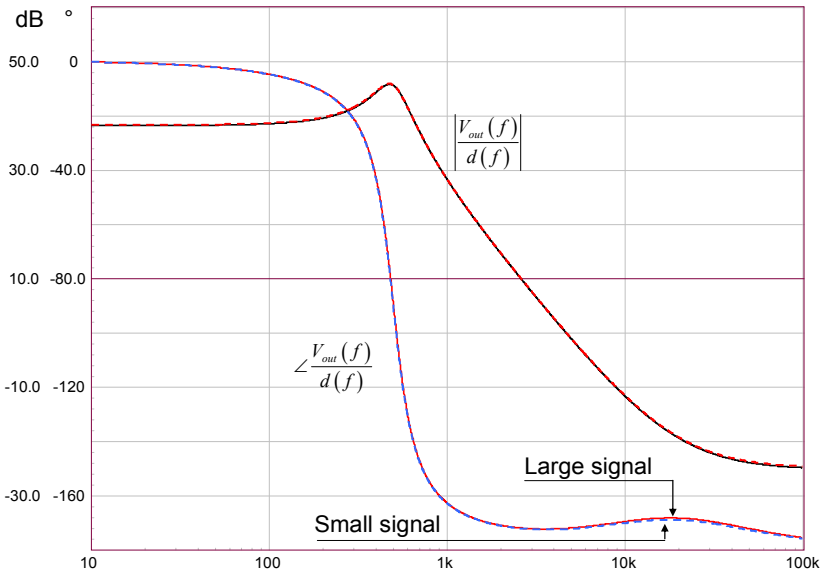


Figure 33: The frequency response of the large-signal model and that of our simplified circuit from **Figure 32** are identical.

Generating the Equations

We start from the inductor current equal to the voltage at node "c" divided by the inductor impedance. The voltage at node "c" is defined by the voltage at node "p" in series with voltage source B_{10}. The voltage at node "p" is simply minus the output voltage reflected to the primary side via the transformer turns ratio N (neglecting the diode forward drop). We have

$$I_L(s)=\frac{V_{(c)}}{sL_p}=\frac{-\frac{V_{out}(s)}{N}+V_{ap}\left[d(s)-d_1(s)\right]D_0+\frac{V_{out}(s)}{N}D_0}{sL_p} \tag{15}$$

Source d_1 can be rewritten since the current in L_p is now defined (it is I(Vc) in the d_1 source from **Figure 32**)

$$d_1(s)=\left[\frac{-\frac{V_{out}(s)}{N}+V_{ap}\left[d(s)-d_1(s)\right]D_0+\frac{V_{out}(s)}{N}D_0}{sL_p}+d(s)\cdot k_{ivd}+d_1(s)\cdot k_{ivd1}\right]k_{d1iv}+V_{out}(s)k_{d1vo} \tag{16}$$

Solving for $d_1(s)$ leads to

$$d_1(s)=\frac{D_0V_{out}(s)k_{d1iv}-V_{out}(s)k_{d1iv}+D_0NV_{ap}d(s)k_{d1iv}+sNL_p\left(V_{out}(s)k_{d1vo}+d(s)k_{ivd}k_{d1iv}\right)}{sNL_p\left(1-k_{d1iv}k_{ivd1}\right)+D_0NV_{ap}k_{d1iv}} \tag{17}$$

The output current is the primary current scaled by the transformer turns ratio N. It is the current defined by source B_7 minus the current flowing in the inductor and defined by (15):

$$I_{out}(s)=\frac{\left[\dfrac{-\dfrac{V_{out}(s)}{N}+V_{ap}\left[d(s)-d_1(s)\right]D_0+\dfrac{V_{out}(s)}{N}D_0}{sL_p}\right](D_0-1)+I_c\left[d(s)-d_1(s)\right]}{N} \tag{18}$$

In this expression, I_c is a dc value already determined in part II of this article series

$$I_c=\frac{V_{out}^{\ 2}}{R_L\cdot d\cdot V_{in}} \tag{19}$$

The I_{out} current circulates in an impedance made of r_C, C_{out} and the load resistance R_L as shown in **Figure 34**.

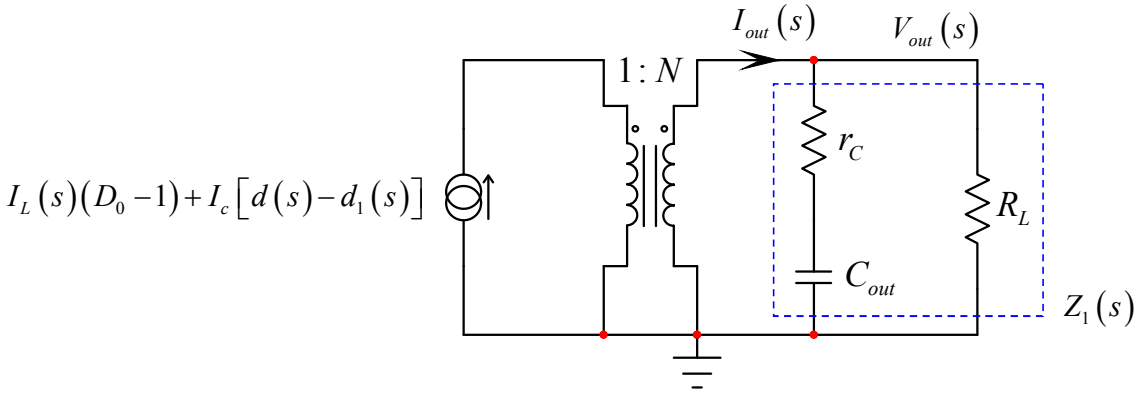


Figure 34: The final representation includes the transformer driving a complex impedance made of the output capacitor, its ESR and the load resistance R_L.

This output current can also be defined as

$$I_{out}(s)=\frac{V_{out}(s)}{Z_1(s)} \tag{20}$$

Impedance Z_1 can be derived quickly either by paralleling r_C + C_{out} with R_L or applying Fast Analytical Circuits Techniques (FACTs). Using either approach, when the result is rearranged you should find

$$Z_1(s)=R_L\frac{1+sr_CC_{out}}{1+s(r_C+R_L)C_{out}} \tag{21}$$

Now combining (18), (20) and (21), we can write

$$\frac{\left[\dfrac{-\dfrac{V_{out}(s)}{N}+V_{ap}\left[d(s)-d_1(s)\right]D_0+\dfrac{V_{out}(s)}{N}D_0}{sL_p}\right](D_0-1)+I_c\left[d(s)-d_1(s)\right]}{N}=\frac{V_{out}(s)}{R_L\dfrac{1+sr_CC_{out}}{1+s(r_C+R_L)C_{out}}} \tag{22}$$

The fun now lies in solving for V_{out} and rearranging the transfer function in a 2nd-order polynomial form. With the help of Mathcad®, we obtain:

$$\frac{V_{out}(s)}{d(s)} = H_0 \frac{\left(1+\frac{s}{\omega_{z_1}}\right)\left(1-\frac{s}{\omega_{z_2}}\right)}{1+b_1 s+b_2 s^2} = H_0 \frac{\left(1+\frac{s}{\omega_{z_1}}\right)\left(1-\frac{s}{\omega_{z_2}}\right)}{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2} \tag{23}$$

in which we have determined the following raw coefficients

$$H_0 := \frac{\left[N_1\cdot\left(k_{ivd}\cdot k_{d1iv}+k_{d1iv}\cdot k_{ivd1}-1\right)\right]\cdot\left[V_{ap}\cdot\left(1-D_0\right)\right]}{\left[\left(2\cdot D_0-D_0^{\,2}-I_c\cdot k_{d1iv}+k_{d1iv}\cdot k_{ivd1}-2\cdot D_0\cdot k_{d1iv}\cdot k_{ivd1}+D_0^{\,2}\cdot k_{d1iv}\cdot k_{ivd1}+D_0\cdot I_c\cdot k_{d1iv}-N_1\cdot V_{ap}\cdot k_{d1vo}+D_0\cdot N_1\cdot V_{ap}\cdot k_{d1vo}-1\right)-\frac{N_1^{\,2}\cdot V_{ap}\cdot k_{d1iv}}{R_L}\right]}$$

$$b_1 := \frac{V_{ap}\cdot\left[N_1^{\,2}\cdot\left[I_p-L_p\cdot k_{d1iv}\cdot k_{ivd1}+V_{ap}\cdot k_{d1iv}\cdot\left(C_{out}\cdot R_L+C_{out}\cdot r_C\right)\right]-R_L\left[C_{out}\cdot r_C\cdot\left(2\cdot D_0-D_0^{\,2}-I_c\cdot k_{d1iv}+k_{d1iv}\cdot k_{ivd1}-2\cdot D_0\cdot k_{d1iv}\cdot k_{ivd1}+D_0^{\,2}\cdot k_{d1iv}\cdot k_{ivd1}+D_0\cdot I_c\cdot k_{d1iv}-N_1\cdot V_{ap}\cdot k_{d1vo}+D_0\cdot N_1\cdot V_{ap}\cdot k_{d1vo}-1\right)+I_c\cdot L_p\cdot N_1\cdot k_{d1vo}\right]\right]\cdot\left(D_0-1\right)}{V_{ap}\cdot\left(1-D_0\right)\left[R_L\left(2\cdot D_0-D_0^{\,2}-I_c\cdot k_{d1iv}+k_{d1iv}\cdot k_{ivd1}-2\cdot D_0\cdot k_{d1iv}\cdot k_{ivd1}+D_0^{\,2}\cdot k_{d1iv}\cdot k_{ivd1}+D_0\cdot I_c\cdot k_{d1iv}-N_1\cdot V_{ap}\cdot k_{d1vo}+D_0\cdot N_1\cdot V_{ap}\cdot k_{d1vo}-1\right)-N_1^{\,2}\cdot V_{ap}\cdot k_{d1iv}\right]}$$

$$b_2 := \frac{\left[D_0\cdot V_{ap}\cdot\left(D_0-1\right)\cdot\left[N_1^{\,2}\cdot\left(C_{out}\cdot R_L+C_{out}\cdot r_C\right)\cdot\left(L_p-L_p\cdot k_{d1iv}\cdot k_{ivd1}\right)-C_{out}\cdot I_c\cdot L_p\cdot N_1\cdot R_L\cdot k_{d1vo}\cdot r_C\right]\right]}{\left[D_0\cdot V_{ap}\cdot\left(1-D_0\right)\left[R_L\cdot\left(2\cdot D_0-D_0^{\,2}-I_c\cdot k_{d1iv}+k_{d1iv}\cdot k_{ivd1}-2\cdot D_0\cdot k_{d1iv}\cdot k_{ivd1}+D_0^{\,2}\cdot k_{d1iv}\cdot k_{ivd1}+D_0\cdot I_c\cdot k_{d1iv}-D_0\cdot N_1\cdot V_{ap}\cdot k_{d1vo}+D_0^{\,2}\cdot N_1\cdot V_{ap}\cdot k_{d1vo}-1\right)-D_0\cdot N_1^{\,2}\cdot V_{ap}\cdot k_{d1iv}\right]\right]}$$

$$\omega_{z1} := \frac{1}{r_C\cdot C_{out}} \qquad \omega_{z2} := \frac{V_{ap}\cdot\left(1-D_0\right)}{\left(I_c\cdot L_p\right)} \qquad Q := \frac{\sqrt{b_2}}{b_1} \qquad \omega_0 := \frac{1}{\sqrt{b_2}}$$

The classical CCM-operated voltage-mode flyback converter transfer function (without leakage inductance) given in the literature follows the form of (23) and uses the below definitions:

$$H_0 = \frac{NV_{in}}{(1-D)^2} \quad \omega_{z_1} = \frac{1}{r_C C_{out}} \quad \omega_{z_2} = \frac{(1-D)^2 R_L}{DL_p N^2}$$

$$Q = \frac{1-D}{N} R_L \sqrt{\frac{C_{out}}{L_p}} \qquad \omega_0 = \frac{1-D}{N\cdot\sqrt{L_p C_{out}}}$$

Testing Analytical Expressions

If we assume the operating values from **Figure 1** and plot the response given by (23) considering either the complicated coefficients with a zero l_{leak} (r_C = 0 Ω) or the simplified flyback expression, both magnitude and phase response plots perfectly superimpose as represented in **Figure 35**.

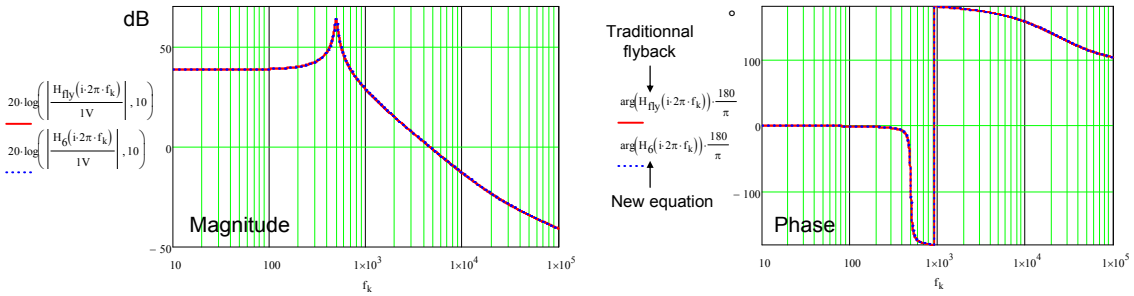


Figure 35: When the leakage inductance is set to 0, the equation with complex coefficients and the traditional flyback expression return the same frequency response plots.

The next test consists of setting l_{leak} to 10 µH and superimposing the plots obtained from Mathcad® and the small-signal SPICE simulation. As shown by **Figure 36**, the perfect superimposition of curves confirms our mathematical derivation of the transfer function considering the leakage inductance.

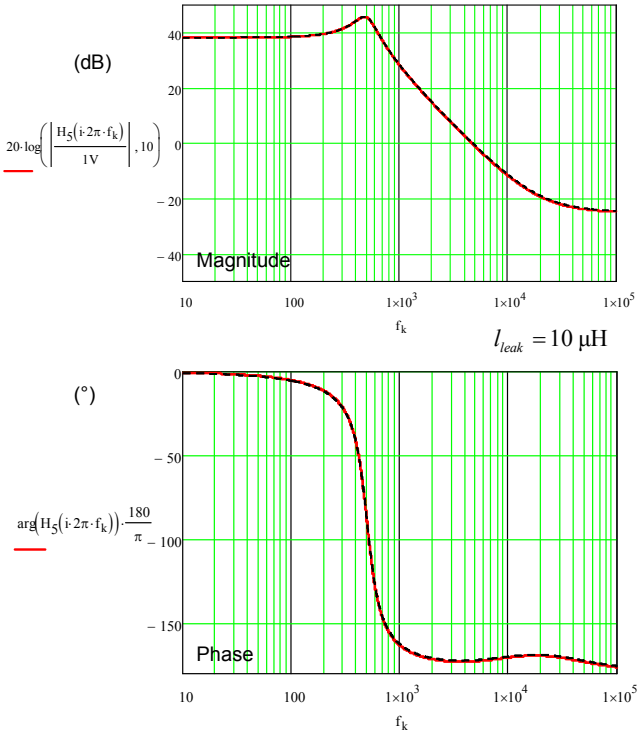


Figure 36: SPICE and Mathcad® plots superimpose perfectly, confirming our analytical derivation of the transfer function linking d to V_{out} in **Figure 29**.

Finally, to compare our modeling approach with another simulation platform, my colleague Dr. Capilla captured the simplified cycle-by-cycle model introduced in part I in a Simplis® template (**Figure 37**) and ran several configurations to extract the small-signal response. Results appear in **Figure 38** over which we have pasted the SPICE simulation results obtained with the small-signal model.

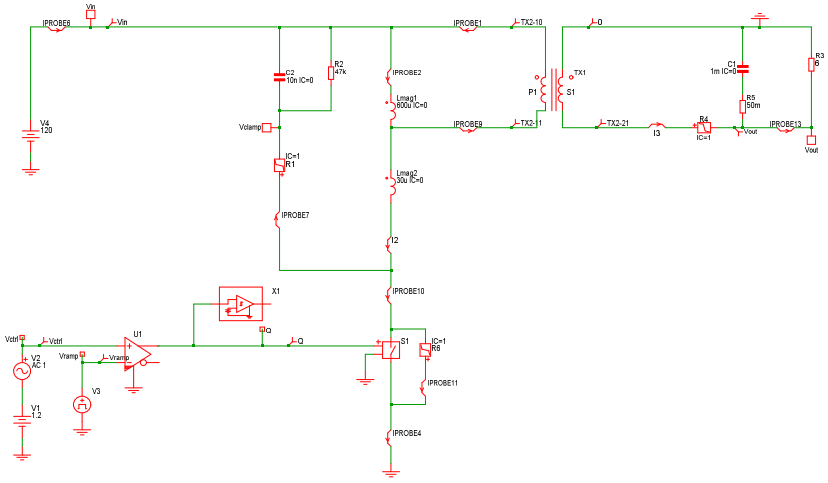


Figure 37: Simplis® can extract the small-signal response from a switching circuit.

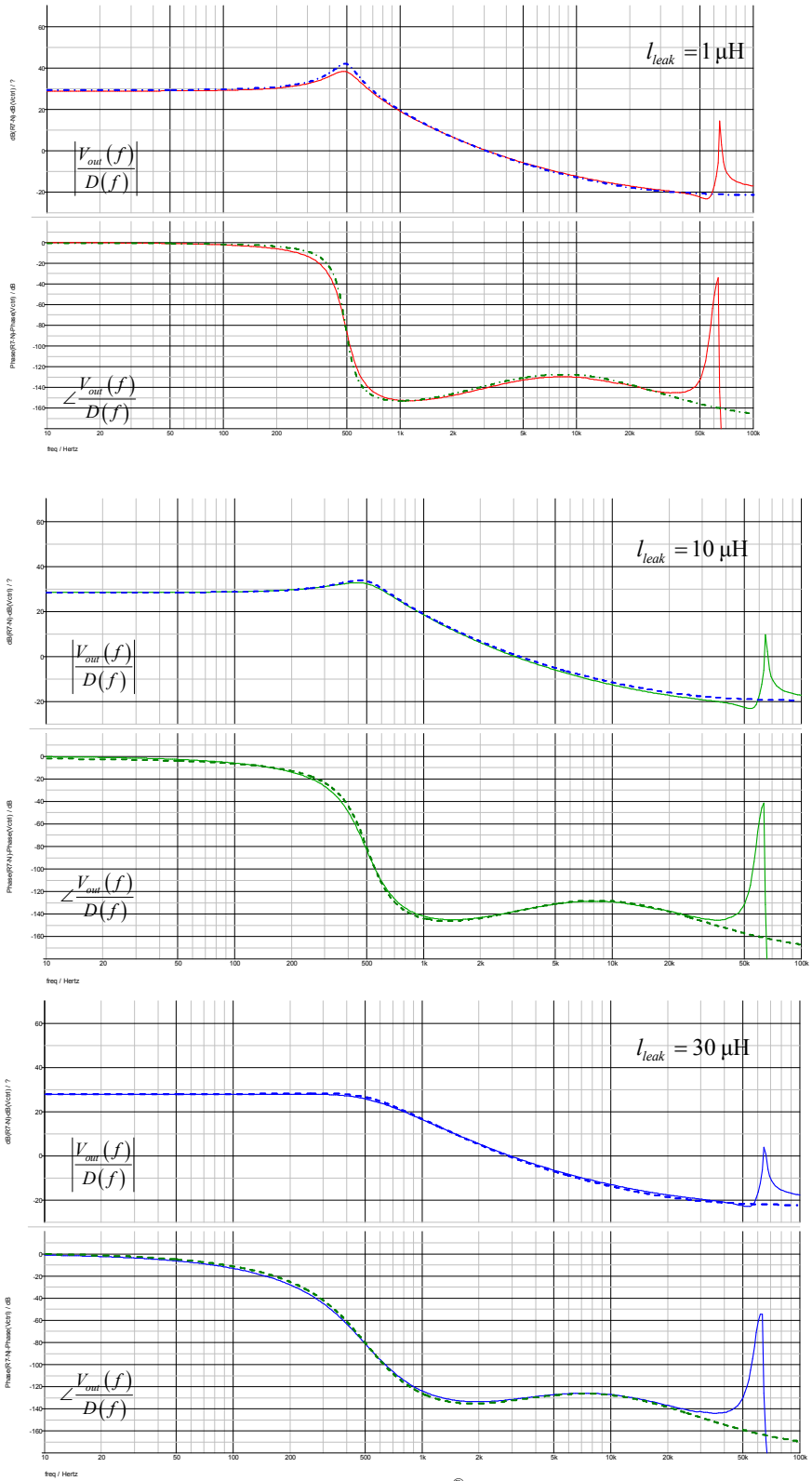
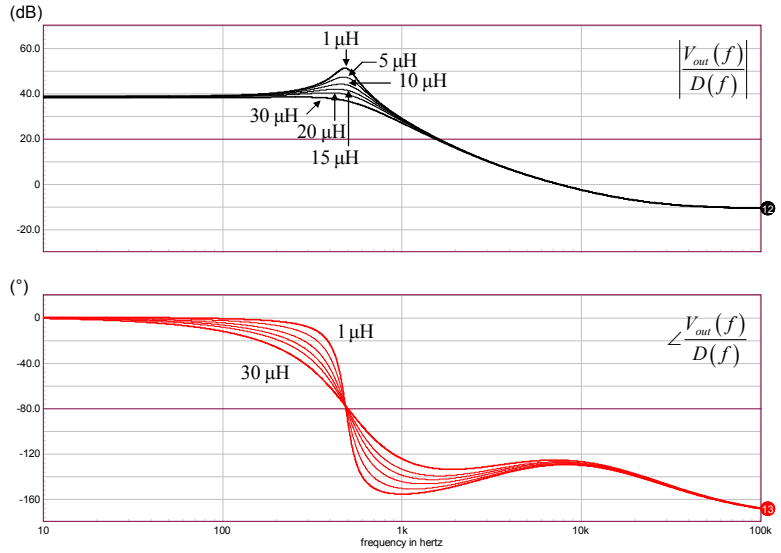


Figure 38: Dynamic responses from Simplis® (solid lines) show a slightly damped circuit compared to the SPICE averaged model (dotted lines).

For the 1-µH leakage inductance value, Simplis® shows a slightly lower Q, probably due to losses inherent to some of the selected switching elements in the simulated circuit. For higher leakage inductance values (10 and 30 µH), the agreement is very good and curves almost superimpose.

Leakage Inductance and Quality Factor

Now that our model is correct, we can ac-sweep **Figure 1** circuit and see how magnitude and phase curves are affected by the leakage inductance. With a low leakage inductance, the Q is significant and exceeds 10 dB. As the leakage inductance grows, more energy is lost per switching cycle and the quality factor weakens. For a large inductance value, 30 µH, the system becomes overdamped.



$D_0 = 40\%$

Figure 39: Increasing the leakage inductance clearly damps the response of the CCM flyback converter operated in voltage mode.

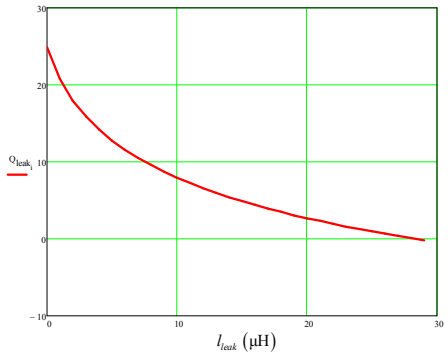


Figure 40: The quality factor in dB reduces as the leakage inductance increases.

In **Figure 40**, we have plotted Q versus the leakage inductance value, confirming its damping effect on the flyback converter.

In current mode, the duty ratio truncation disappears because despite the inclusion of the leakage inductance, the peak current remains unaffected as t_{on} naturally expands to meet the peak setpoint. As written in [1], it is possible to show that the switch duty ratio in current mode control (CCM) is defined by

$$d = \frac{F_{sw}\left(V_c - R_i I_c\right)}{S_a + \frac{V_{ac} R_i}{2\left(L_p + l_{leak}\right)}} \tag{24}$$

In which F_{sw} is the switching frequency, V_c is the control voltage, R_i the sense resistance, I_c the current in terminal "c" as defined by (6), S_a the external compensation ramp in V/s and V_{ac} the voltage between terminals "a" and "c". Despite the increase of the leakage inductance, the effective duty ratio (the switch duty ratio reduced by the leakage inductance magnetization time) remains fairly constant. As such, it is mostly the delay in the secondary current that affects the output voltage. However, the output voltage reduction in current mode control is still lower than that of the voltage mode converter (**Figure 41**).

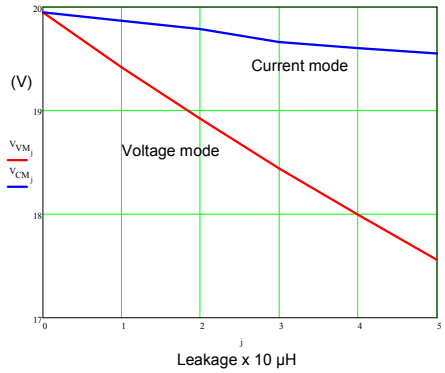


Figure 41: In current mode, the peak current remains constant and the on-time naturally expands to compensate for the leakage inductance presence. As a result, the output voltage is almost unaffected unlike in voltage-mode control.

Conclusion

In this final part, we have expressed the control-to-output transfer function of the CCM flyback converter operated in voltage mode. The leakage inductance increases the dissipation in the clamping source and provides damping of the frequency response: classical equations do not predict this behavior and a new model had to be derived. Further to a linearization process, a new small-signal transfer function has been established, showing the leakage inductance effect on the quality factor. Current mode control however, is less affected by the leakage inductance. References [2] and [3] point to papers recognizing the influence of the leakage element without formalizing its effect in an updated transfer function expression.

The leakage inductance small-signal effects in a classical hard-switching converter are not of great importance. However, analyzing mechanisms at work paves the way for the study of a more complex architecture, the active clamp flyback converter. In this structure, the leakage inductance is purposely used to defeat switching losses inherent to the drain-source lumped capacitance. As we will see in a next series of articles, duty ratio truncation increases as the leakage inductance current no longer starts from 0 but from a negative value.

References

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