Linking the cross over frequency and the output voltage undershoot

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In most power supplies design examples, it is common to arbitrarily place the cross over frequency to one fifth or one tenth of the switching frequency. However, it is little known that the cross over frequency actually affects the output impedance of the converter and a relationship actually exists between both variables. Therefore, once the capacitor has been selected based on its operating parameters such as rms current, temperature or acceptable voltage ripple, the designer can analytically select his cross over frequency to match the desired output undershoot. This article shows how to derive the relationship which links both parameters and will help you to tailor the bandwidth to exactly fit your needs.

A simplified buck converter

Figure 1 represents a simplified buck converter associating a square-wave generator to a low-pass filter. Both the inductor and the capacitor are affected by ohmic losses. The output impedance of such a network can easily be derived once the input source is shorted:

$$Z_{out} = \left(sL_{out} + r_{Lf} \right) \| \left(r_{Cf} + \frac{1}{sC_{out}} \right) \tag{1}$$

By inspection, we can see that the inductor resistive path dominates the impedance in dc (L_{out} is shorted and C_{out} is open) to let the inductor enter the picture as the frequency increases. Then, the capacitor impedance starts to take over until it becomes a short circuit and leaves the impedance value to its series loss r_{Cf}.

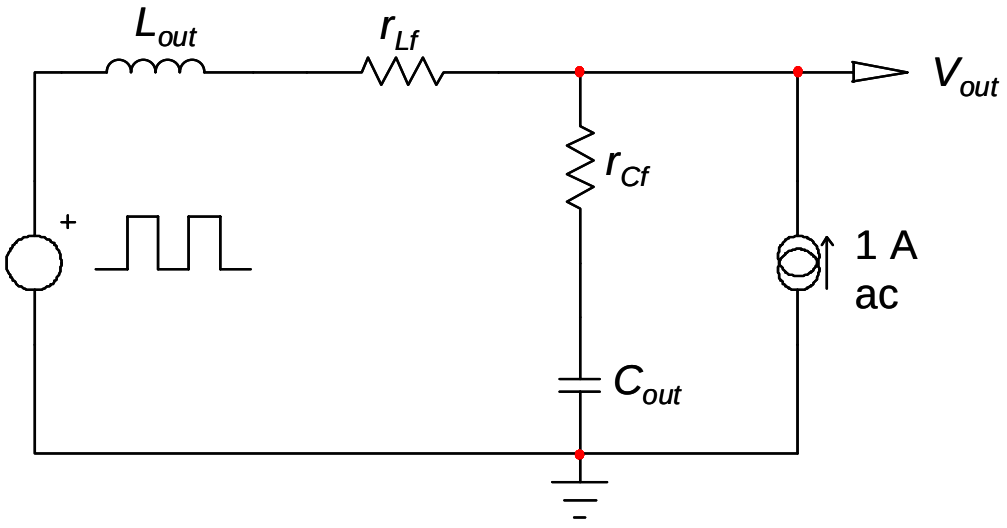

Figure 1: a simplified buck representation where the current source ac sweeps the output impedance.

By connecting an 1-A ac source to the output, we have the ability to quickly plot the output impedance versus frequency using a SPICE simulator. Figure 2 portrays the obtained results. As we can see, a peaking occurs at the resonant frequency f_0. The maximum of this peaking can be analytically derived, as shown in Ref. [1]:

$$Z_{out,\max} = \frac{{Z_0}^2}{R_{Lf}} \sqrt{1 + \left(\frac{R_{Lf}}{Z_0} \right)^2} \tag{2}$$

Where $Z_0 = \sqrt{\frac{L_{out}}{C_{out}}}$ is the characteristic impedance of the filter. Such peaking is typical of a buck output impedance behaviour where the *LC* filter has been optimized to minimize the losses. This situation induces a

high quality coefficient, hence a severe peaking in the impedance graph. One of the feedback aims is to minimize the output impedance to reduce as much as possible the voltage drop when a load step occurs. On this plot, the natural output impedance of the filter dramatically peaks at the resonant frequency. Therefore, if we select a cross over frequency below the *LC* filter resonance, we will not have enough gain to get rid of the resonance and, despite a good phase margin, the system will oscillate. If we want to obtain a good transient response, we have to make sure the loop gain remains high enough to tame the peaking when it occurs. In other words, the cross over frequency f_c must be selected at least three-five times above f_0.

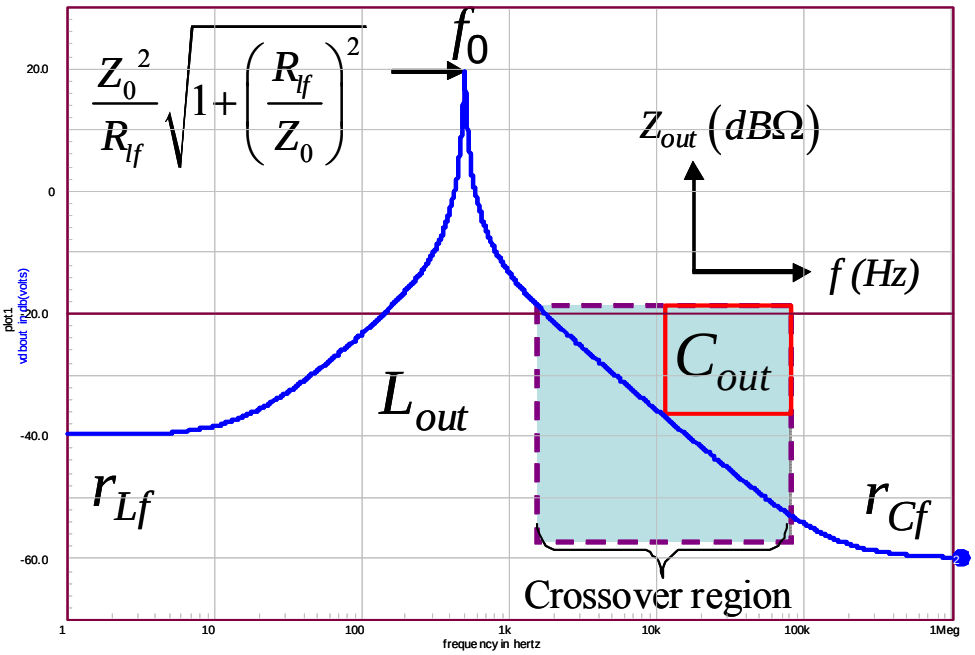

Figure 2: as shown by Eq. (1), the ohmic losses dominate the output impedance at both extremes of the graph ($f = 0$ and $f = \infty$)

In Figure 2, if we select a cross over region beyond the resonance, we can see an impedance graph dominated by the output capacitor impedance C_{out}. At the cross over frequency, this impedance is:

$$Z_{out,OL}(f_c) \approx \frac{1}{2\pi f_c C_{out}} \tag{3}$$

Above the cross over frequency, the capacitor ohmic losses dominate the output impedance of the network. To make sure Eq. (3) rules the output impedance alone at the cross over point, the capacitor Equivalent Series Resistor (ESR) must be much smaller than this impedance at the cross over frequency. Mathematically, the following condition must be met:

$$r_{C_f} << \frac{1}{2\pi f_c C_{out}} \tag{4}$$

The final capacitor choice, besides ripple current and temperature considerations, will also include a consideration for the capacitor ESR at the selected cross over frequency.

Closing the loop

Any voltage generator can be pictured with an equivalent circuit associating a dc source V_{th} and an output resistor R_{th}, according to French telegraph engineer, Charles Thévenin (1857-1926). V_{th} is evaluated by measuring the output voltage on a unloaded converter and R_{th} is found by measuring the output voltage difference in two loading current conditions. Imagine that Figure 3a depicts an open-loop buck converter using Figure 1 approach. Once loop control is installed through a compensator bringing gain and phase boost as in

Figure 3b, the open-loop impedance transforms into a closed-loop output impedance which now obeys the following law (Figure 3c):

$$Z_{out,CL}(s) \approx Z_{out,OL}(s)\frac{1}{1+T(s)} \tag{5}$$

Where:

$Z_{out,OL}$ is the open-loop output impedance before the feedback is applied.

$Z_{out,CL}$ is the closed-loop output impedance for a loop gain $T(s) = H(s)G(s)$.

We now have an output impedance whose value depends on the open-loop gain. In dc, for s = 0, we assume a large loop gain to ensure a good dc regulation. In other words, the feedback brings the open-loop impedance to a very low value. On the contrary, when the frequency increases, the gain reduces and when the cross over point is reached, the gain no longer acts upon the output impedance. Mathematically, this can be written as follows:

$$\lim_{s\to 0}\left|Z_{out,CL}(s)\right| \approx 0 \tag{6}$$

$$\lim_{s\to s_c}\left|Z_{out,CL}(s)\right| \approx \left|Z_{out,OL}(s)\right| \tag{7}$$

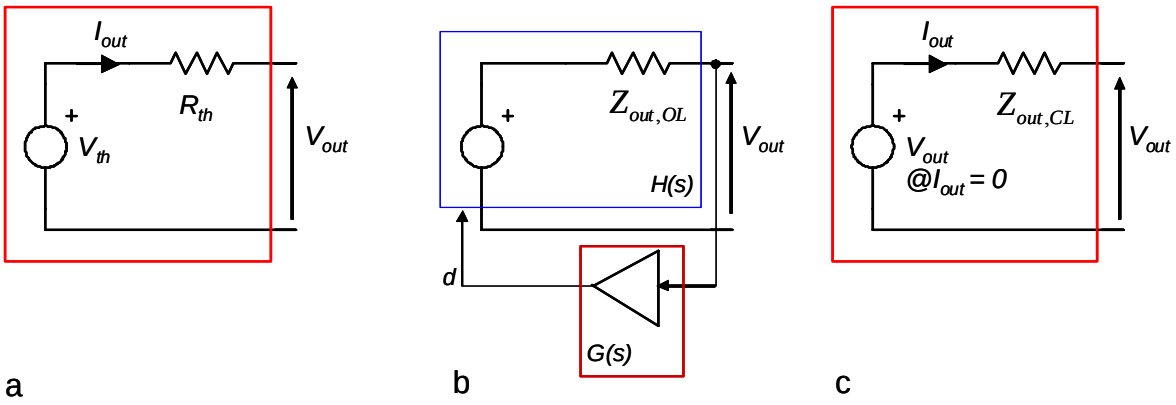

Figure 3: implementing loop control on a converter improves several parameters among which the output impedance.

If we use a SPICE average model and compensate a voltage-mode buck converter, we have the possibility to ac sweep its output impedance as we did in Figure 1. Looking at the output impedance graph (Figure 4), it shows what Eqs. (5)(6) predicted: in the low frequency domain, thanks to a high open-loop gain, the output impedance remains extremely small $\left(r_{Lf}/\left|T_0\right|\right)$ but as the frequency increases, we start to see the inductive behaviour. Then, at the cross over point, the loop gain reaches 0 dB and both the open-loop and closed-loop impedance are almost equal to the output capacitor impedance given by Eq. (3).

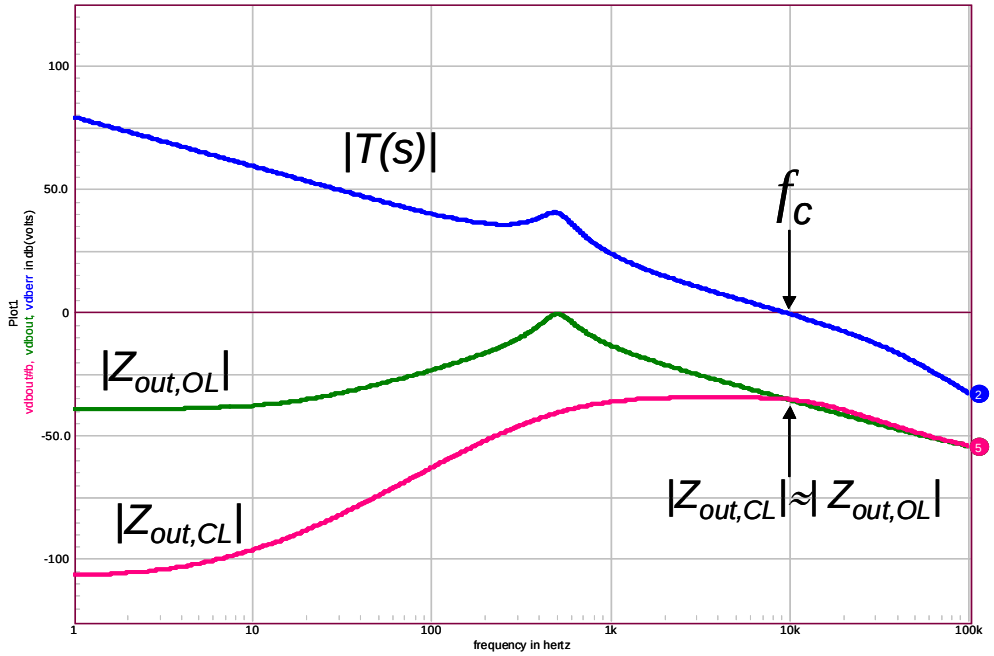

Figure 4: the output impedance is low in dc but rises with frequency as an inductive element would do.

Deriving an approximate output impedance definition

In the above lines, we have used the term "almost" to compare the open and closed-loop output impedances at the cross over frequency. However, let us try to see how close they are in the vicinity of the cross over point. To calculate the module of the Eq. (5) right term, $\frac{1}{1+T(s)}$,there are several methods. One of them consists in applying a sinusoidal modulation to the complete chain made of the converter transfer function *H(s)* followed by the compensator transfer function *G(s)*. This is exactly what we would do in the laboratory to explore the true open loop response of our compensated converter. However, in this particular case, rather than expressing the modulation signal via a classical form $\hat{A}\sin(\omega t+\varphi)$, we will use a phasor notation where φ represents the phase lag brought by the total chain when stimulated at the cross over frequency. This is what Figure 5 details where a 1-V modulation is assumed.

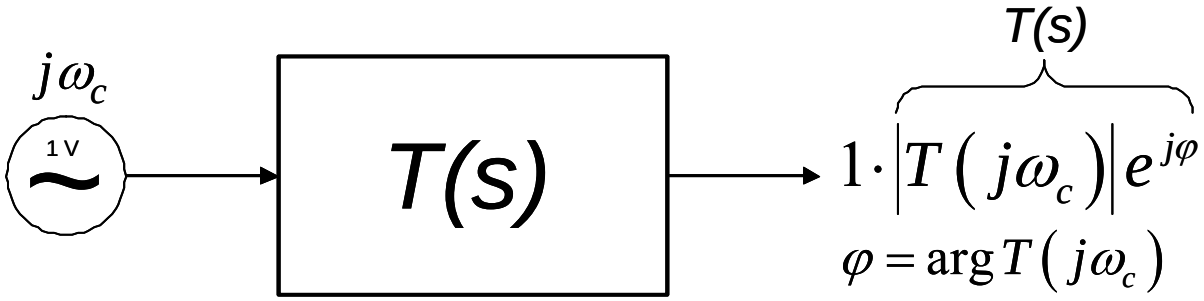

Figure 5: a sinusoidal signal can also be represented by a rotating vector expressed using the Euler notation.

The phasor notation can be updated using Euler's formula as Eq. (8) shows:

$$T(s)=\left|T(s)\right|e^{j\varphi}=\left|T(s)\right|\left[\cos(\varphi)+j\sin(\varphi)\right] \tag{8}$$

In this equation, the term φ relates to the phase difference between the output signal and the input modulation. A design criteria for us is not φ but φ_m, our phase margin. To help linking both terms together, Figure 6 shows the contribution of the loop to the total phase lag.

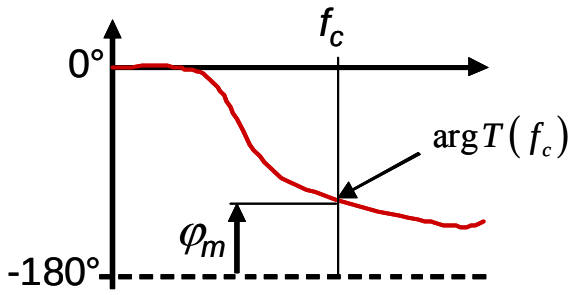

Figure 6: the phase margin is the distance between φ and the –180° axis.

Based on the figure, we can write:

$$-180 = \arg T(j\omega_c) - \varphi_m \tag{9}$$

Solving for φ, we have:

$$\varphi = \arg T(j\omega_c) = \varphi_m - 180 \tag{10}$$

Based on the above equation, we can update Eq. (8):

$$\left|T(j\omega_c)\right| e^{j\varphi} = \left|T(j\omega_c)\right|\left[\cos(\varphi_m - 180) + j\sin(\varphi_m - 180)\right] = \left|T(j\omega_c)\right|\left[-\cos(\varphi_m) - j\sin(\varphi_m)\right] \tag{11}$$

Knowing that the loop gain module at cross over is 1, then T(s) can be approximated to be:

$$T(s) = -\cos(\varphi_m) - j\sin(\varphi_m) \tag{12}$$

Based on this result, we can now update Eq. (5) as follows:

$$\left|Z_{out,CL}(s)\right| = \left|Z_{out,OL}(s)\right|\left|\frac{1}{1+T(s)}\right| = \left|Z_{out,OL}(s)\right|\left|\frac{1}{1-\cos(\varphi_m) - j\sin(\varphi_m)}\right| \tag{13}$$

Solving this equation leads to:

$$\left|Z_{out,CL}(s)\right| \approx \frac{1}{2\pi f_c C_{out}} \frac{1}{\sqrt{2-2\cos(\varphi_m)}} \tag{14}$$

As we can see, the module of the capacitor impedance is now affected by a term dependent upon the phase margin. We can now plot the variations of this term versus the phase margin as proposed by Figure 7.

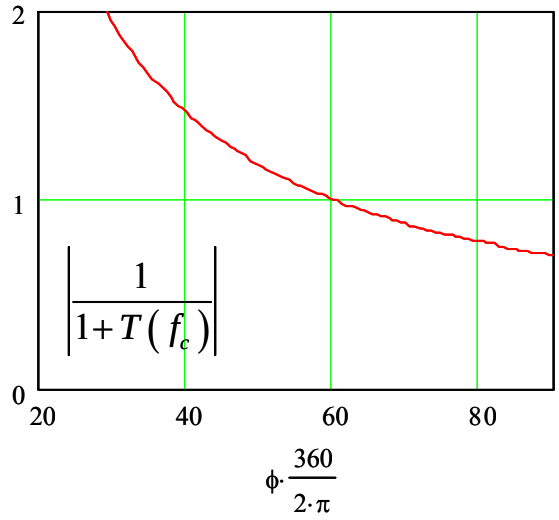

Figure 7: the phase margin degrades the output impedance below 60°.

As observed, a phase margin below 60° degrades the output impedance of the converter and it slightly improves it above.

A design example

Let us assume we have a power supply where the output capacitor is 1000 µF. This choice has been made by the designer considering the voltage output ripple conditions and the corresponding rms current circulating in the capacitor. The specification asks us a maximum voltage drop of 80 mV when the converter undergoes a current step ΔI_{out} of 2 A. What bandwidth do we need to reach this parameter? If we use Eq. (3) and apply a 2-A step, we can predict the voltage drop by:

$$\Delta V_{out} \approx \frac{\Delta I_{out}}{2\pi f_c C_{out}} \tag{15}$$

From this equation, it is easy to extract the minimum cross over point:

$$f_c \approx \frac{\Delta I_{out}}{\Delta V_{out} C_{out} 2\pi} = \frac{2}{80m \times 1m \times 2\pi} = 4\ kHz \tag{16}$$

Based on this result, we must check that the capacitor ESR is lower than:

$$Z_{C_{out}} @ 4\ kHz = \frac{1}{2\pi \times 4k \times 1m} = 40\ m\Omega \tag{17}$$

We found that a 1000-µF capacitor from the Panasonic FM series could be the right choice. From the manufacturer data-sheet, the component features an ESR of 19 mΩ at 100 kHz. This ESR alone will contribute to a drop of $19m \times 2 = 38\ mV$ which is 47% of our specification. To offer some margin in our design, we will increase the cross over frequency to 6 kHz and purposely compensate our converter to meet this goal. Once compensated, our 5-V voltage-mode buck converter loop gain Bode plot SPICE simulation appears in Figure 8. It shows a cross over frequency of 5.8 kHz together with a rather comfortable phase margin of 76°. The output voltage drop is now going to split between the capacitor and its ESR term. Based on a 76° phase margin, we can approximate the capacitive contribution by using Eq. (14):

$$\Delta V_{out,C} \approx \frac{2}{6.28 \times 5.8k \times 1m} \frac{1}{\sqrt{2 - 2\cos(76)}} = 2 \times 27.4m \times 0.812 = 44.5\ mV \tag{18}$$

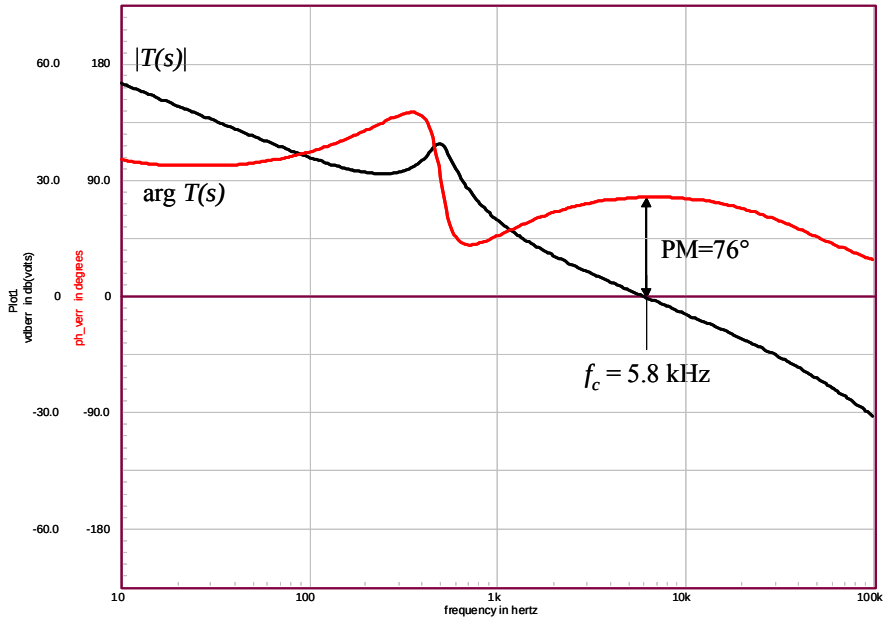

Figure 8: the compensation leads to a cross over frequency of 5.8 kHz with a phase margin of 78°.

We are now going to step load the output by a current source ranging from 100 mA to 2.1 A in a 10-µs time frame. The simulation results are shown in Figure 9. We can see that the total output undershoot is well within our design goals with a theoretical 53.5-mV deviation. The ESR spike is 35 mV and lasts only during the output current circulation in the capacitor. The capacitive contribution reaches 50 mV, in a fairly good agreement with Eq. (14) predictions.

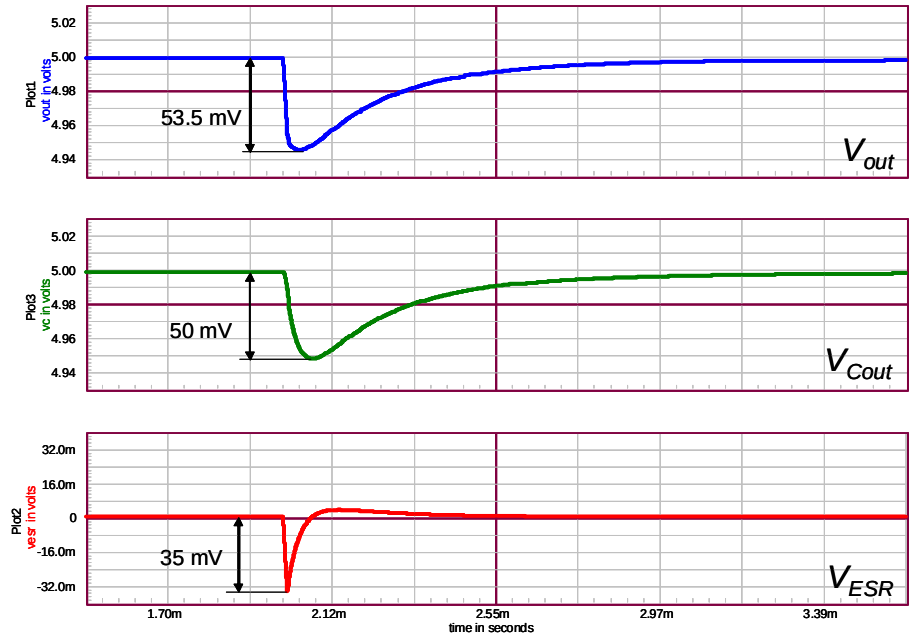

Figure 9: the 2-A step load gives an undershoot well under control.

As can be seen, the ESR term amplitude depends on the current step undergone by the output. When the load change is slow enough, the loop has a means to attenuate the ESR contribution. However, most of the time, the transient loading conditions are so fast that all the current step translates into a voltage spike over the ESR. Given its steepness, the loop cannot fight it. The situation degrades further if the output current rate of change reaches high values, like in motherboard applications for instance. In that case, the inductive term called the

Equivalent Series Inductance (ESL) of the capacitor starts to enter the picture and the situation worsens. In these extreme cases, the capacitor selection is almost solely based on the contribution of its parasitic terms and no longer on its capacitive value.

Conclusion

This article has shown the link between the cross over frequency and the converter undershoot in response to a load step. The designer can now analytically select a cross over frequency rather than arbitrarilly chosing it based on the switching. If the capacitor impedance plays a role in relationship with the selected cross over frequency, there are other terms whose contribution is out of control. These are the ESR and the Equivalent Series Inductor (ESL) of the output capacitor. They are respectively sensitive to the output current step and the current slope. As loop control has almost no influence on their contributions, it is the designer task to make sure these parasitic terms stay low enough to keep the overall transient response within the original specifications.

References

1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill, 2008